Front-end Electronics for the ATLAS Tile Calorimeter

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Abstract

The ATLAS Tile Calorimeter readout is designed to measure energy depositions in a single cell from ~30 MeV to 2 TeV. Signals up to 800pC must be processed over a dynamic range of 16 bits. More than 10,000 channels of front-end readout electronics are needed for this detector. This paper presents the design of the front-end readout electronics and its test results.

1. Introduction

The ATLAS Tile Calorimeter (TileCal) must measure signals from energy depositions in a single cell which range from ~30 MeV to 2 TeV. This corresponds to signals up to 800 pC from each of the two photomultipliers associated with a cell. In addition, the calorimeter response and electronics gain must be calibrated and monitored with a precision of better than 1%. This paper deals particularly with the pulse shaping, calibration and control electronics for the version of the electronics used in test beam running in 1998 (Version 2.3). It is very close to the final one.

2. Front-end Electronics Design

Most analog functions of the front-end electronics are contained on a 7-cm by 4.7-cm printed circuit board, called the 3-in-1 card, located inside the steel shield of each PMT block.

The 3-in-1 card provides the following functions:

- shaping of the PMT pulse to match the requirements of the 10-bit 40MSPS digitizers
- production of two linear outputs with relative gain of 64 to achieve an overall dyanamic range of 16 bits
- production of an analog signal for the Trigger Summation Card of the Level 1 trigger
- charge integration for monitoring and calibration of the calorimeter cells
- calibration of response by injection of a known charge over the full dynamic range of the system.

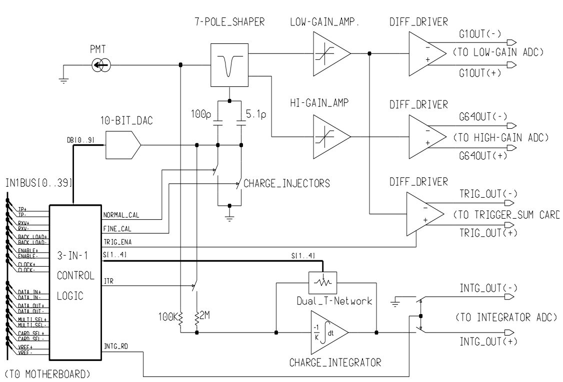

Fig. 1: Block diagram of front-end electronics.

A block diagram of the system is shown in Figure 1.

Bi-gain Analog Circuitry

A bi-gain readout system has been developed. Shaped PMT signals are produced with a gain ratio of 64 and are sent to high-gain and low-gain digitizing ADCs. The maximum signal from the high-gain channel corresponds to 1/64 of 800pC, and the signal clamps for higher inputs. This output is encoded with a 10-bit ADC. Thus one count corresponds to 12.2fC. The low-gain channel has a relative gain of one and covers the entire 800pC range with a second 10-bit ADC. The two channels together provide a 16-bit dynamic range measurement over the 800pC scale. The resolution of a single channel is most limited at the cross over point between scales and corresponds to 3%, for a noise on the low gain scale of 0.5 counts. Since the calorimeter energy to be measured is the sum of many channels this resolution does not impact the quality of the final measurement.

The advantage of this bi-gain approach is that the signal is processed by an easily calibrated linear system with a good resolution. The analog signals are AC coupled to the continuously operating 40MSPS digitizers and any baseline shift can be directly measured and subtracted with negligible impact on the resolution. The schematic of the bi-gain readout channel is shown in Figure 2.

The current-source nature of the PMT and its fast pulse makes it attractive to use a purely passive shaper. Filters have been designed to satisfy a range of restrictions on their transfer functions. A Bessel filter has a transfer function optimized to obtain a linear phase response[3]. It is attractive in this application since its impulse response has only a tiny oscillatory behavior. A fast 7-pole passive shaper based on Bessel filter characteristics has been developed. The 7

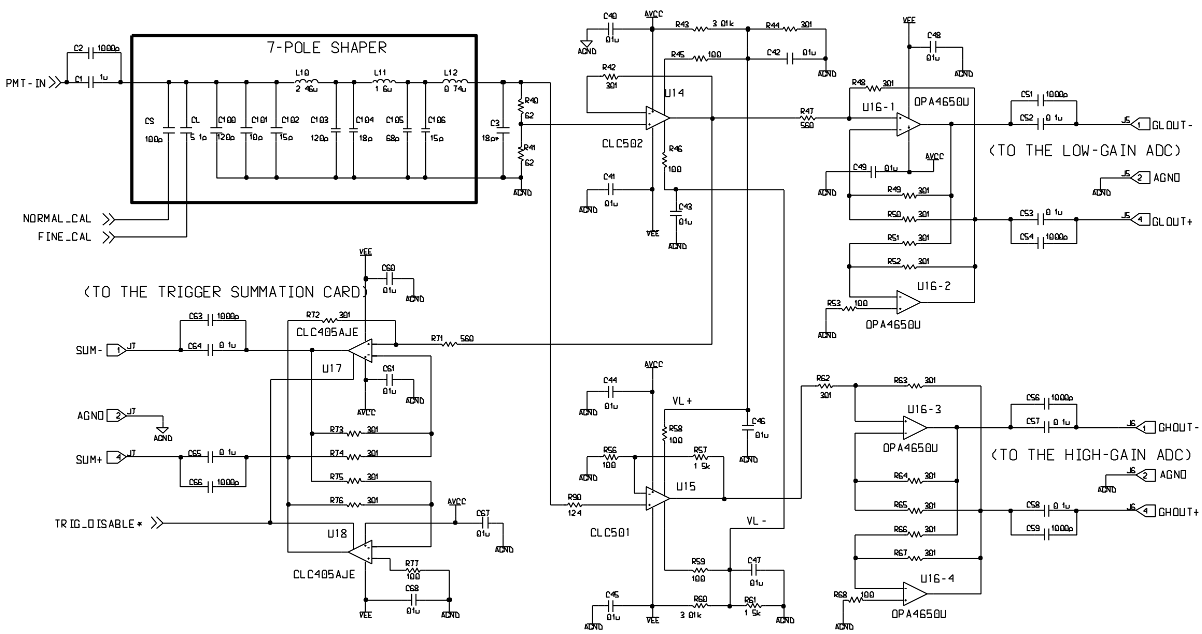

Fig. 2: Bi-gain analog circuit.

poles provide a fast settling time and a reduced noise bandwidth[3]. A single pole device has an effective noise bandwidth of 136% of the break frequency while 7 poles have a noise bandwidth of 115% [4,5,6,7]. The impedance of this shaper is 124 ohms and the bandwidth at -3db is 12Mhz. It provides outputs for the two gain ranges with sensitivities of 1V/800pC and 2V/800pC. This reduces the amplifier gain needed for the high-gain channel and hence improves the signal-to-noise ratio. The amplifier contribution dominates the output noise of high-gain channel.

The high-gain channel uses a gain-of-16 clamping amplifier followed by a unity gain differential driver to a 100Ω 10-cm-long shielded twisted-pair cable. The maximum output is 1V (± 500 mV differential) corresponding to a full scale input signal of 12.5pC. The low-gain channel consists of a unity-gain clamping amplifier and a gain of 1/2 differential driver. This channel receives a signal from the shaper low sensitivity output (1V/800pC), and produces a full scale output into the 100Ω cable of 1V (± 500 mV differential) for a full scale input signal of 800pC input.

Comlinear CLC501 and CLC502 are used as clamping amplifiers for the high-gain and the low-gain channels respectively. The CLC502 is a unity-gain stable amplifier. Both amplifiers are high speed current-feedback op amps with output voltage clamping. This protects the system against overdrive. It prevents damage to downstream circuitry and reduces the dead time due to amplifier saturation. The high-gain channel has a recovery time of 3ns for an input overdrive of a factor of 32.

The output drivers employ the Burr-Brown OPA4650. It is a quad, low power, wide band voltage feedback op amp and is used in a cross-coupled differential configuration[8]. This gives a high common mode rejection and complementary outputs. The differential gain is set by a single resistor ratio (R48/R47 for the low-gain channel, R63/R62 for the high-gain channel and R72/R71 for the trigger signal). There is no need for side-to-side resistor matching with gain changes as is the case for conventional differential amplifiers.

Trigger summation driver

The 3-in-1 card provides a differential signal to a Trigger Summation Card, mounted in the electronics drawer on the motherboard. This card performs an analog sum of signals belonging to an individual calorimeter trigger tower. The sum must have a 10-bit dynamic range[9]. This signal is derived from the low-gain output of the card. Its cross-coupled differential output driver is based on the Comlinear CLC405 which has a TTL-compatible disable control. The disable function is provided to prevent faulty behaviour of an individual PMT or electronics card from spoiling the output of an entire calorimeter tower. While disabled, the CLC405 exhibits a high input/output impedance. The typical off isolation is 59db. Its quiescent power is 8mW compared to its enabled power of 35mW.

Charge Integrator

This circuit is designed to measure photomultiplier current induced by a radioactive source used to calibrate the calorimeter, as well as the current from minimum bias proton-proton interactions at the LHC. The integrator is a low pass DC amplifier with 6 gain settings, one calibration input and a switchable output. It uses a JFET input op amp (LF411) with a resistive and capacitive feedback to define the integration time constant and the DC transimpedance of the circuit. A schematic of the circuit is shown in Figure 3.

Because the dynamic range of the minimum bias current varies with position of the cell in the calorimeter and with the luminosity of the LHC, a programmable transimpedance is required to maintain an adequate resolution. The gain is chosen so that the smallest expected minimum bias current will produce 40 counts from the 12-bit ADC, thus allowing current measurements with a minimum resolution of 2.5%. During cesium source calibrations, a resolution better than 1% is achieved. The integrator requires a transimpedance as high as 100MΩ. This infers a very high impedance feedback resistance. Since the largest SMD resistance commonly available is 20 MΩ and we cannot rely on the printed circuit board to exhibit such low leakage, the feedback network was configured as a programmable dual T-network. The value is programmable through the communication interface of the 3-in-1 card. The gains are 7.5M, 20M, 27.5M, 54.3M, 72.9M and 100M. The smallest transimpedance value is set by the largest calorimeter cell minimum bias current at LHC design luminosity, with a margin of 1.5 for higher currents.

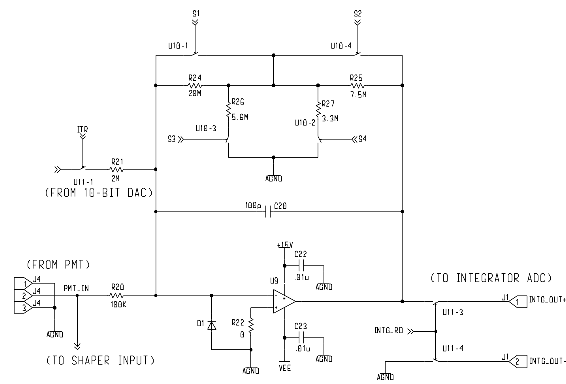

Fig. 3: Charge integrator.

The PMT is DC coupled to the integrator through a 100KΩ resistor to measure the average DC current. The equivalent source impedance seen from the integrator input must be as large as possible to minimize the offset voltage at the integrator output. The bi-gain shaper is AC coupled PMT and presents a relatively low impedance (124Ω) at high frequencies. A cutoff is thereby introduced in the frequency response of the integrator, higher than the one needed for calibration purposes. The capacitive feedback of the integrator fixes the time constant at 10ms for the highest gain, giving a ripple of less than one LSB of 12-bit ADC for cesium calibration. The non-linearity is less than 0.3%.

The output of the integrator is connected to a bus on the 3-in-1 mother board with an analog switch operated by a remote controller. The signal on the bus is digitized by one ADC in each super drawer. Thus, there are a maximum of 48 integrators per ADC.

Electronics Calibration

Each electronics channel must have a relative calibration better than 1% to avoid degrading the overall resolution. A charge injection system is used for this purpose. The schematic is shown in Figure 4. Two calibration inputs are used to cover the wide dynamic range of the system. A 10-bit DAC receives a low noise, high precision, reference voltage

(4.096V) with extremely low temperature coefficient (0.5ppm per ℃) from the mother board. A precise output driver with a gain of 2 boosts this voltage to 8.192V to charge the injection capacitors. A controllable timing pulse (TP) closes the discharge switch for either normal or fine calibration. The normal calibration capacitor is 100pF with a precision of 0.5%. This allows the injection of a signal of 800pC for an 8V DAC setting. The fine calibration capacitor is 5.1pF and provides a maximum charge of 40pC. This small capacitor is calibrated using the larger one. The charging time constants are 1ms and 5us for the normal and fine capacitors.

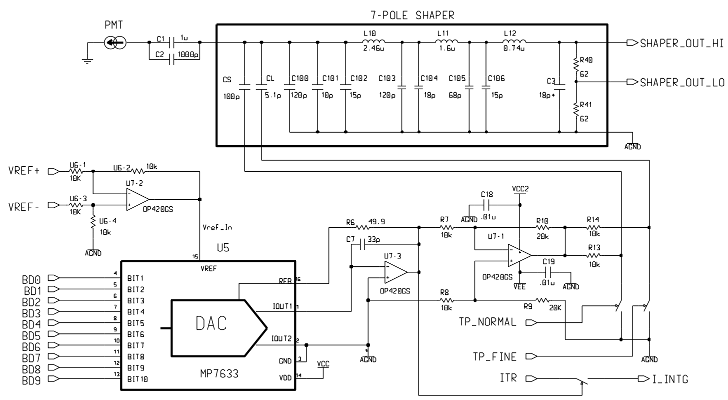

Fig. 4: Electronics calibration system.

Calibration is also provided for the integrator. The 10-bit DAC applies a known negative voltage (to -4.096V) to a 2MΩ precision resistor. This serves as a reference current source for the integrator.

3-in-1 Bus and Control Logic

Digital control of the 3-in-1 cards is needed for the charge injection calibration, to control the gain of the charge integrator, to control the switching of the charge integrator output onto the analog bus, and to enable/disable the trigger summation output. The control signals are supplied by a mother board which runs the length of the electronics drawer. A dedicated serial RS-422 differential digital bus is used for communication with the 3-in-1 cards. The RS-422 protocol provides a good noise immunity, together with an excellent speed and long distance transmission capability. The digital control logic is impemented with an Altera EPM7064 EPLD. The connection between the 3-in-1 card and mother board is through a high density 40-position connector and a 1mm-pitch ribbon cable.

Simulation and Test Results

Both frequency and time domain simulations have been performed.

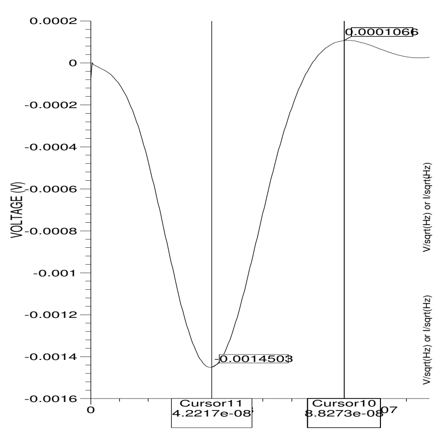

Fig. 5: Impulse response.

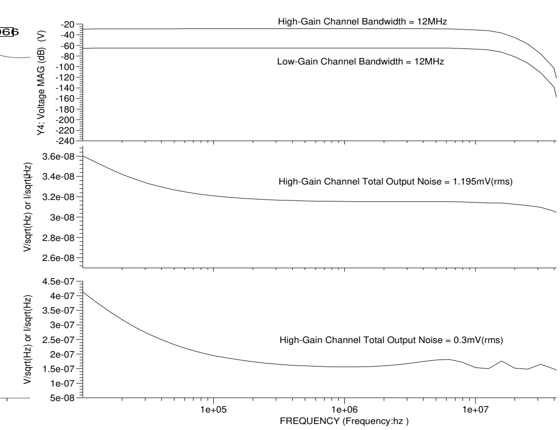

Fig. 6: Bandwidth and noise.

The frequency domain simulations include the shaper impulse and step response, the bandwidth of each output and the noise. The simulation result of the shaper impulse response is shown in Figure 5. It has small oscillatory behavior with a 7% overshoot and FWHM of 35ns. The bandwidth of both high-gain and low-gain channels and their output noise distributions are shown in Figure 6. Both channels have a bandwidth of 12Mhz at -3db. The total output noise is 1.2mV (rms) and 0.3mV (rms) for high-gain and low-gain outputs respectively.

Time domain studies include simulations with the expected PMT input signal and simulations of the charge injection

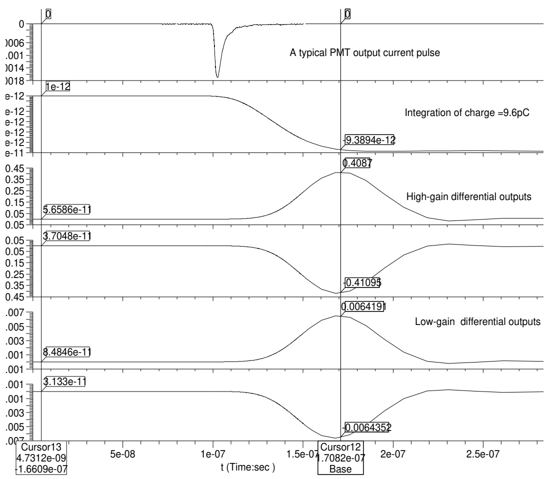

Fig. 7: Response to a 9.6pC input.

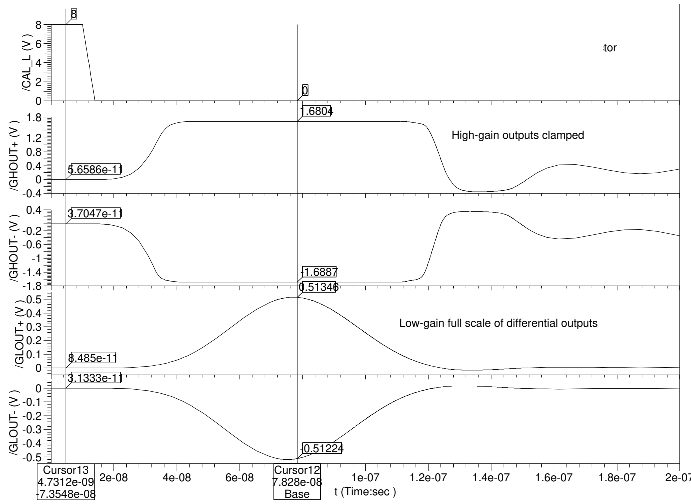

Fig. 8: Response to a full scale 800pC input.

calibration system. Figure 7 shows the outputs for a 9.6pC PMT signal. Figure 8 shows the response for an 800pC signal injected by the normal calibration capacitor. The high-gain output is clamped and the low-gain channel has a full scale response.

Specialized simulations have been performed to study the sensitivity of the output pulse shape to component tolerances and to variations in the shape of the input current pulse.

(1) Dependence of output shape on component tolerance
The shaper is an LC network of 10 capacitors with a tolerance of ±1%, 3 inductors with a tolerance of ±5% and 2 resistors with a tolerance ±1%. The result of 99 Monte-Carlo simulation runs in which component values are varied within their tolerances are shown in Figure 9. The peak output amplitude varies by less than 0.3%.

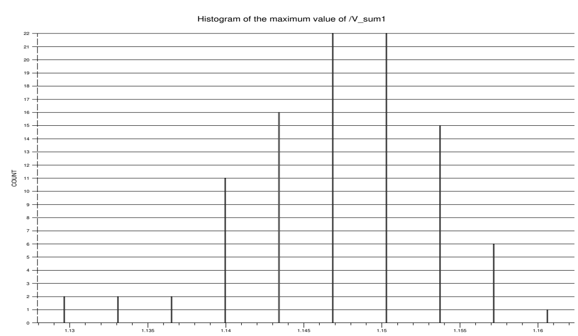

Fig. 9: Histogram of output amplitudes for 99 simulations.

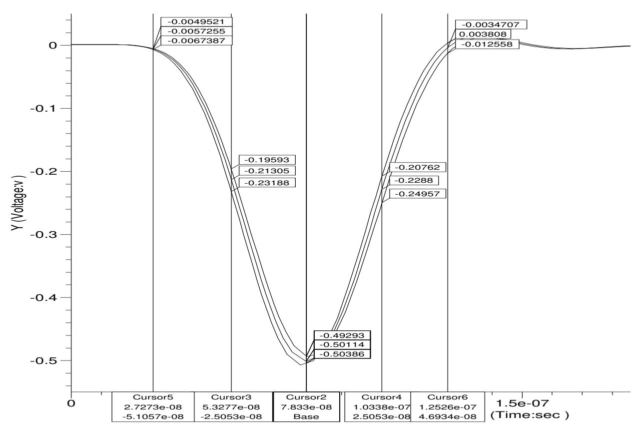

Fig. 10: Variation in output shape with input width.

(2) Dependence of output shape on input pulse width
Event-to-event fluctuations occur in the energy deposition processes in the calorimeter. Because of this there is the potential for variations in the width of the PMT signal. The typical PMT pulse is 18ns FWHM with a 5ns rise time. A sweep simulation has been run by setting 200pC input current pulses, with a rise time of 4ns and fall times of 16ns, 20ns and 24ns respectively. The result is shown in Figure 10. Changes in the peak amplitude are at the level of ±1%

for ±20% changes in signal fall time. Changes in the integral output signal are considerably less and, if necessary, corrections can be applied based on the digitized samples at ±25 ns from the peak.

To measure the overall performance of the system the charge injection calibration system was used. The 3-in-1 output signals were delivered to a 40MSPS 10-bit VME ADC module. To set the timing of the injected signal relative to the digitizing clock a large signal was injected and the timing was varied in steps of ~185ps in order to center a digitization on the peak of the 3-in-1 output pulse.

To measure the system linearity, the magnitude of the peak sample was recorded and the charge injection signal was varied over a wide range of amplitudes. For each input charge setting, 25 injections recorded and averaged. Figure 11 shows the linearity and the deviation from a straight line fit. Both the high and the low-gain channels show deviations from linearity well below the level of one count.

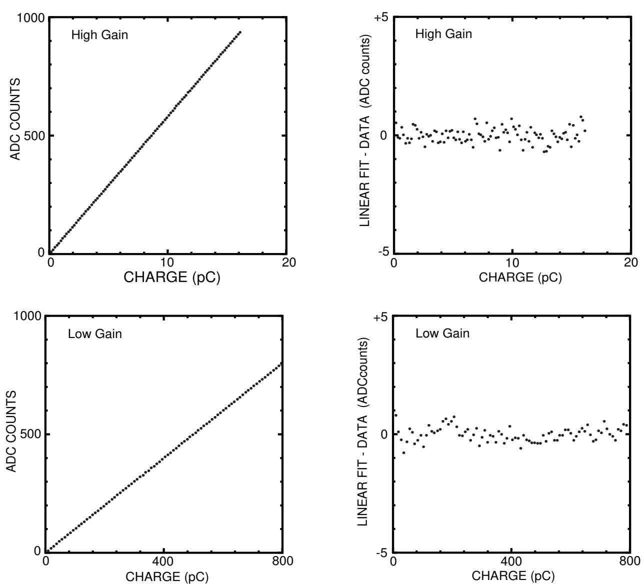

Fig. 11: High gain and low gain linearity.

For each charge injection event, 10 digitizations outside the signal region were used to measure the pedestal and its RMS. The pedestal stability can be characterized on the 250ns time scale of individual events as well as on the millisecond time scale between events. For individual events the RMS values are 0.75 counts and 1.3 counts for the low-gain and high-gain signals respectively. The SPICE simulation described above predicts 0.3 counts and 1.2 counts if the only noise source is the 3-in-1 card itself. The measurements are consistent with an additional noise contribution of ~ 0.7 counts and is largely attributable to the digitizer. This result is entirely satisfactory for the planned application. Over millisecond time scales the pedestal RMS values are 0.4 and 0.35 counts for high and low gain respectively.

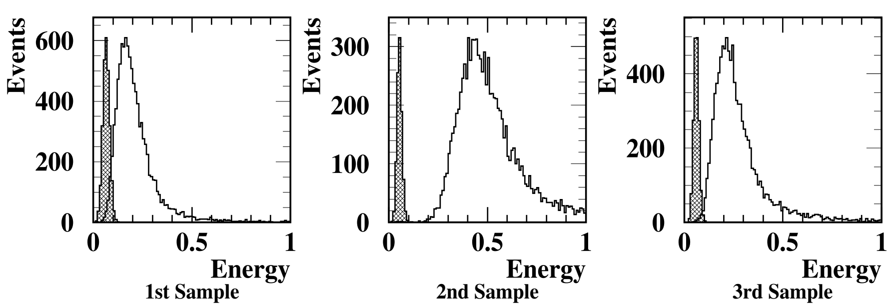

Fig. 12: TileCal response to muons for the three sampling depths.

This bi-gain electronics system was used for test beam studies in 1997 and 1998. Figure 12 shows the measured response to muons from the three sampling depths of the calorimeter. The electronic noise of the readout system can be seen from the shaded pedestal distributions near zero. For all three depths the width of the muon signal is substantialy larger than the electronic noise indicating that the electronics contribution is negligible.

The calorimeter resolution and linearity have also been studied using charged pions and protons. The system performance using the electronics described here is excellent and exceeds the design specifications.

4. Conclusions

A novel pulse shaping circuit using only passive components has been designed to exploit the current source capablility of the TileCal photomultipliers. This shaper has been combined with a slow integrator, a charge injection calibration system, and a digital control system on a small printed circuit board to be located at each of the PMTs. The performance of the system has been studied with SPICE simulations and with prototype tests using both charge injection signals and test beam measurements. Excellent results were achieved.

For 1998 test beam work a set of 120 prototype bi-gain cards were built with the characteristics described above. The system was tested with the first version of the digitizer system located in the TileCal electronics drawers, as well as with 10-bit digitizers located in VME crates.

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