Interface card specification
(Version 0.99)

Interface card (version 0.99) has passed the test beam run. This note describes the basic aspects of the current version of the card, The data format has been updated since version 0.9. This was accomplished with the existing hardware but a revision of the firmware in the EPLD.

A. Features of current version:

1. Serial in and Parallel out.
2. Integrated GLINK LSC card, working at 20 bits, 40MHz mode, data rate 640Mbit/s.
3. Dual channel readout redundancy.
4. Full insensitivity to timing of individual input signals relative to TTC clock.
5. Recorded data to correspond to physical geometry of channels.
6. Provide 17 TTC LVDS signal with automatic selection from two TTC fiber inputs, 9 of which is delivered by 3 pin connectors and 8 of which go through the foil connectors to each digitizer board.
7. Prototype of current version has passed the radiation test.

B. Data format(2 samples):

Recall that each DMU handles 3 PMT channels and produces the following data words:

Tile-DMU data format:(32bits)

0	**P**	**Data channel 1 (10 bits)**	**Data channel 2 (10 bits)**	**Data channel 3 (10 bits)**

The data output over the S-LINK has the following form in a case of 2 samples per channel:

Word	Contents
1.	**Control word (0x11111110)**
2.	**Data word (32 bits) : D1 ---- Header from DMU1 (see below)**
3.	**D2 ---- 1st data from DMU1**
4.	**D3 ---- 2nd data from DMU1**
5.	**D4 ---- CRC word from DMU1**
6.	**D5 ---- Header from DMU2**
7.	**D6 ---- 1st data from DMU2**
8.	**D7 ---- 2nd data from DMU2**
9.	**D8 ---- CRC word from DMU2**
10.	**D9 ---- Header from DMU3**
11.	**D10 ---- 1st data from DMU3**
12.	**D11 ---- 2nd data from DMU3**
13.	**D12 ---- CRC word from DMU3**
14.	**D13 ---- Header from DMU4**
15.	**D14 ---- 1st data from DMU4**
16.	**D15---- 2nd data from DMU4**
17.	**D16---- CRC word from DMU4**
18.	**D17 ---- Header from DMU5**
19.	**D18 ---- 1st data from DMU5**
20.	**D19---- 2nd data from DMU5**
21.	**D20---- CRC word from DMU5**
22.	**D21 ---- Header from DMU6**
23.	**D22 ---- 1st data from DMU6**
24.	**D23---- 2nd data from DMU6**
25.	**D24---- CRC word from DMU6**
26.	**D25 ---- Header from DMU7**

D26 ---- 1st data from DMU7
D27---- 2nd data from DMU7
D28---- CRC word from DMU7
D29 ---- Header from DMU8
D30 ---- 1st data from DMU8
D31---- 2nd data from DMU8
D32---- CRC word from DMU8
D33 ---- Header from DMU9
D34 ---- 1st data from DMU9
D35---- 2nd data from DMU9
D36---- CRC word from DMU9
D37 ---- Header from DMU10
D38 ---- 1st data from DMU10
D39---- 2nd data from DMU10
D40---- CRC word from DMU10
D41 ---- Header from DMU11
D42---- 1st data from DMU11
D43---- 2nd data from DMU11
D44---- CRC word from DMU11
D45 ---- Header from DMU12
D46---- 1st data from DMU12
D47---- 2nd data from DMU12
D48---- CRC word from DMU12
D49 ---- Header from DMU13
D50 ---- 1st data from DMU13
D51---- 2nd data from DMU13
D52---- CRC word from DMU13
D53 ---- Header from DMU14
D54 ---- 1st data from DMU14
D55---- 2nd data from DMU14
D56---- CRC word from DMU1
D57 ---- Header from DMU15
D58 ---- 1st data from DMU15
D59---- 2nd data from DMU15
D60---- CRC word from DMU15
D61 ---- Header from DMU16
D62 ---- 1st data from DMU16
D63---- 2nd data from DMU16
D64---- CRC word from DMU16
Control word (0xFFFFFFF0)

Note: CRC words are deserialized as other data words.

P means odd parity calculated for all 32 bits.

Tile-DMU Header format is: (32bits)
1plllles drvvvv0m mgggbbbb bbbbbbbb

The header starts with bit 31 set to "1" indicate a header. The other bits as follows:

p
-
Parity (odd)
l
-
Derandomizer length (number of samples).
e

-

Parity error. A parity error was detected from the memory in the last readout.

s

-

SEstr Single Error Strobe recieved from the ttc.

d

-

DEstr Double Error Strobe recieved from the ttc.

r

-

Register parity. Parity from the registers in the chip.

v

-

Variable parity. Parity from the variables in the chip.

0

-

Not used. (Set to 0)

m

-

Mode.

00 - Normal mode
01 - Calibration mode
10 - Test mode
11 - Not used

g

-

High/low gain. Indicates high(1) or low(0) amplification from the 3-in-1 cards.

b

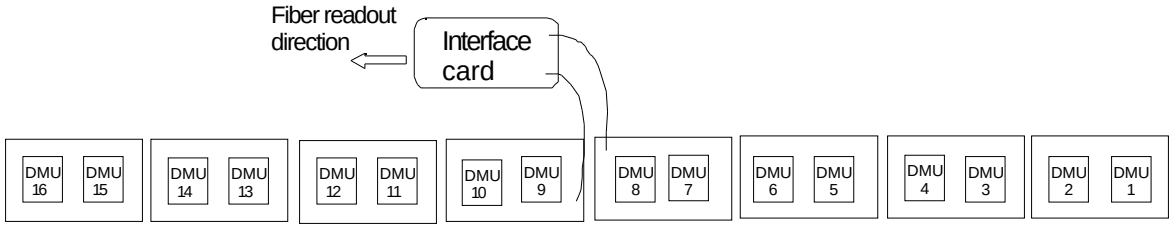
-

Bunch Crossing.

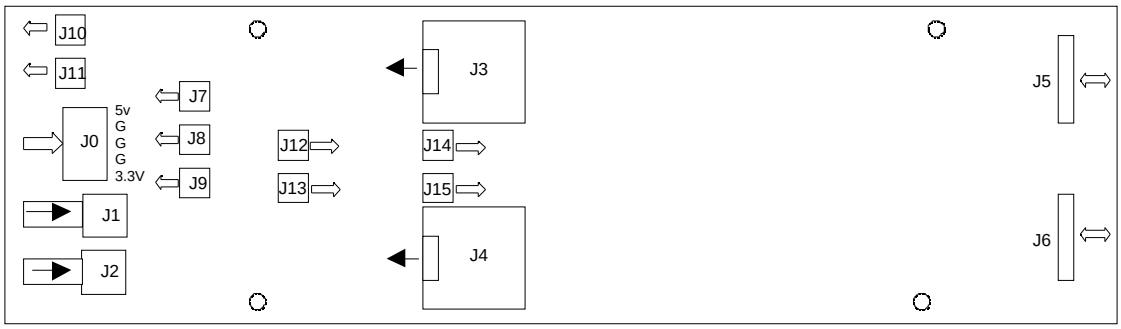
C. Requirements

1. Power: 5V/2.5A .
2. LDC card: GLINK simplex LDC card. PCB version: EP 680-1110-850-A, with modified VHDL version.

D. DMU map

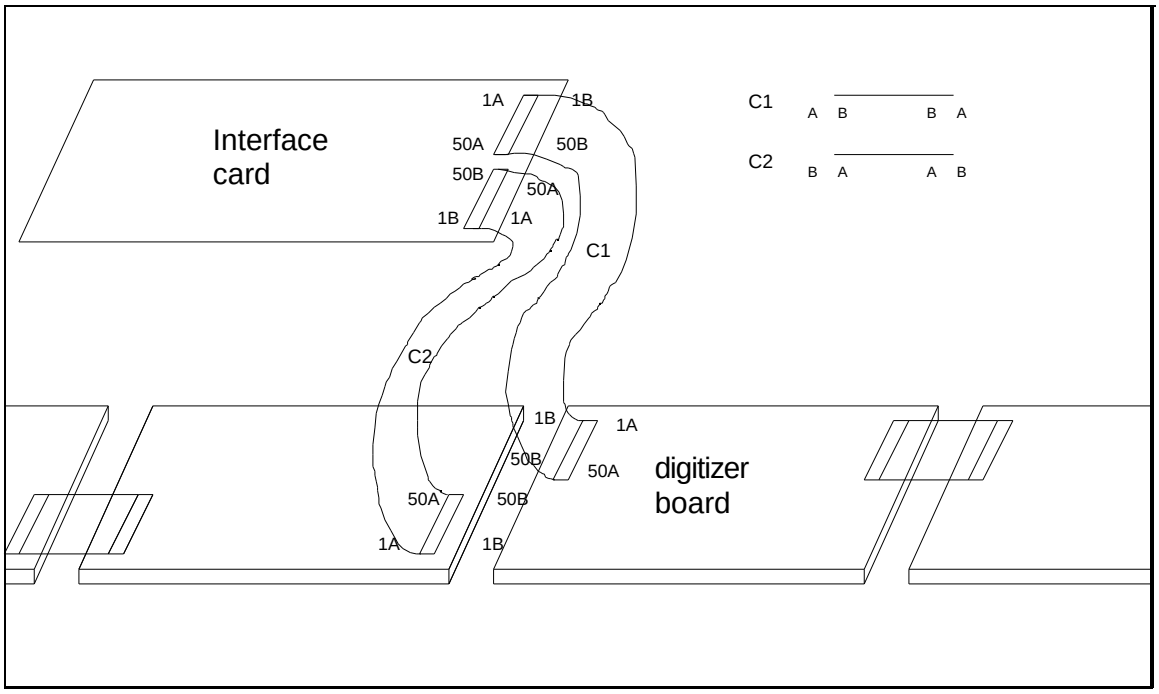


E. Interface card placement



J0: Power connector for 3.3v and 5v.
J1, J2: TTC optical receiver.
J3, J4: Methode optical transceiver for slink.
J5, J6: 100 pin connectors to the digitizer boards.
J7 -- J15: 9 3-pin BERG connectors for delivering TTC signals.

G. Connection between Interface board and digitizer boards



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