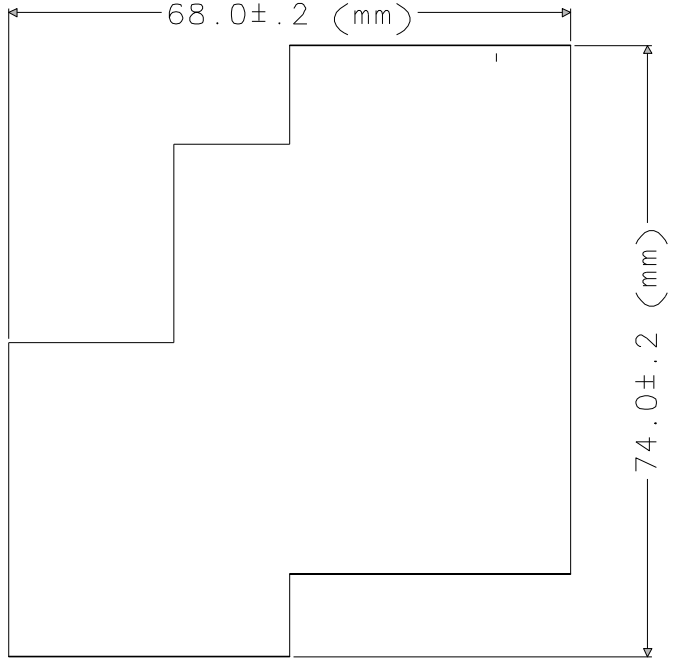
B2428(V3.1B) Board Size (mm)



BOARD SPECIFICATIONS

1. Board Layers: 8

2. Layer Stack Order:
   - Layer1 (Film1): Top component layer(Signal_1).
   - Layer2 (Film2): Power plane(Power,VCC).
   - Layer3 (Film3): Power plane(GROUND).
   - Layer4 (Film4): Inner signal layer(Signal_3).
   - Layer5 (Film5): Inner signal layer (Signal_4).
   - Layer6 (Film6): Power plane (AVCC).
   - Layer7 (Film7): Power plane (AGND).
   - Layer8 (Film8): Bottom component layer(signal_2).

3. Apply solder mask over bare copper on both side:
   Film9: Top solder mask.
   Film10: Bottom solder mask.

4. Apply silkscreen on both side:
   Film11: Top silkscreen.
   Film12: Bottom silkscreen.

5. Material: FR4.
6. Board thickness: 0.062'' +/- 0.010.
7. All layers are equal thickness.
8. Copper thickness 1oz before plating.

9. Ni/Au (chem plated) over bare copper
10. All layers mininum trace width/clearence 0.005"/0.006"

11. All dimensions are in inches unless otherwise noted.

BOARD's DRILL SCHEDULE (inch)

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.012	144	YES	---
⊞	.015	196	YES	---
⌀	.02	45	YES	---
⊟	.028	80	YES	---
⊖	.041	2	YES	---
◫	.13	2	YES	---

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SCHM# 2427V3.1B
SPEC# 2428V3.1B
ASSM# 2429V3.1B

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
B2428 Specification Drawing

SHEET 1 OF 1
DATE 2/26/2001
DRAWN TANG

B- 2428
REV 3.1B