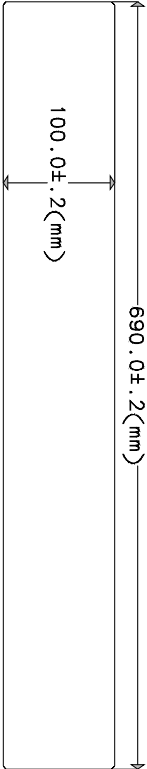


B2316 V3.1 PCB Specifications

B2316 V3.1 Specification Drawing



- (1) Board Layers: 8
- (2) Layer stack order:
- Layer1 (Film1): Top component layer (Signal_1)
- Layer2 (Film2): Power plane (VCC2)
- Layer3 (Film3): Power plane (VCC), (2oz copper)
- Layer4 (Film4): Power plane (GROUND), (2oz copper)
- Layer5 (Film5): Inner signal layer (Signal_3)
- Layer6 (Film6): Inner signal layer (Signal_4)
- Layer7 (Film7): Power plane (VEE)
- Layer8 (Film8): Bottom component layer (Signal_2)
- (3) Apply solder mask over bare copper on both side:
- Film9: Top solder mask (solder_mask_1)
- Film10: Bottom solder mask (solder_mask_2)
- (4) Apply silkscreen on both side:
- Film11: Top silkscreen (Silkscreen_1)
- Film12: Bottom silkscreen (Silkscreen_2)
- (5) Material: FR4 with Tg> 170C
- (6) Board thickness: 0.062'' +/- 0.010''
- (7) All layers are equal thickness.
- (8) Layer2 (VCC) and Layer3 (GROUND) use 2oz copper before plating, other layers use 1oz copper before plating.
- (9) All dimensions are in inches unless otherwise noted.

(10) PCB fabrication meets IPC-6012: Class 2

(11) Bow and Twist: Not exceed 0.75%, Test methods meet IPC-TM-650, L=100mm

BOARD's DRILL SCHEDULE (Inch)

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.015	596	YES	---
⊞	.02	15	YES	---
⊘	.035	560	YES	---
⊞	.046	40	YES	---
⊘	.059	14	YES	---
⊞	.13	4	YES	---
⊕	.14	10	YES	---

(12) Contact person:

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SCHM# B2315 V3.1
SPEC# B2316 V3.1
ASSM# B2317 V3.1

UNIVERSITY OF CHICAGO ELECTRONICS DEVELOPMENT GROUP		
TITLE B2316 V3.1 Specification Drawing		
SHEET DATE DRAWN	1 OF 1 5-12-2000 TANG	B-2316 REV 3.1