subadr   ttcdata

| 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 |

data field

fcode

3in1 flag = 11

fcodes
0000 - set tp
0001 - set tube
0010 - set multi_sel
0011 - set rxw
0100 - set back_load
0101 - load can out register
0110 - reset state machine
0111 - reset CAN

1xxx - command to 3in1
 000 - set intg_rd
 001 - set itr
 010 - set s1-4
 011 - set mse
 100 - enable small C
 101 - enable large C
 110 - set the dac
 111 - enable trig output

COMMANDS EXECUTED IN THE DRAWER LOGIC

TP control   subadr=11000000 data=0000000x   x=0 or 1
  This is the charge injection line which is timed relative to Desclock40Des
   When x=1, the selected U8 switch is opened starting the charging of Cl or Cs
  the charge injection capacitors (see enable small and large C below).
  When TP goes low, charge is injected and the shaping network on the 3in1
  card returns to normal configuration.
  Note: TP can also be controlled with short format broadcast commands which
  is the preferred method since there is some latency in decoding and executing
  the long format commands.

Set TUBE   subadr=11000100 data=tube number (1 to 48)
  This raised the card_sel (card select) line for the specified 3in1 card. Cards ignore
  commands unless they are selected, or are setup for multiselect mode.

Set MULTISEL subadr = 11001000 data=00000x x=0 disable multiselect
                                                x=1 enable multiselect
    With multiselect high (x=1) all cards with there MSE bit set (see below)
    will execute subsequent commands. (see INTG_RD exception)

Set RXW subadr=11001100   data=0000000x   x=0 normal mode
                                                x=1 circular shift on readback
    You will not need this command. It allows readback of a 3in1 card shift
    register without destroying its contents.

Set BACK_LOAD   subadr=11010000 data=0000000x x=0 normal
                                                x=1 load status
  when x goes high, the addressed 3in1 card loads its shift register with
  bits showing the internal status of the card. See cardchk.c for details
 of the bits.

LOAD CAN OUTPUT REGISTER subadr=11011000 data=0000000x
                                                x=0 normal level
                                                x=1 load register
  As a 13 bit command is sent from the drawer logic to a 3in1 card, the current
  contents of the card_sel selected 3in1 card is shifted back to the drawer.
  On the rising edge of x=1, this data is transferred to a register which is
  readout via the ADC card through CANBUS. This is used to read back
  the status (for example) that is loaded with BACK_LOAD.
  (See cardchk.c for how this works).

RESET STATE MACHINE subadr=1101100 data=0000001
                                                x=0 normal
                                                x=1 reset
Resets the drawer card state machine (FPGA code). You probably will not need.

RESET CAN subadr=1101110 data=000000x   x=0 return to normal (reset line low)
                                                x=1 reset line high
  controls the reset line going to the integrator ADC card.

Set INTG_RD subadr=11100000 data=0000000x x=0   U13 switched closed
                                                       x=1   U13 switched open
This command controls the integrator output switch on the 3in1 card. Since only one card can be allowed to drive the bus at a time, card_sel must be set high also. This command ignores the MSE bit.

Set ITR subadr=11100100 data=0000000x x=0 U11 switch is closed
                                                       x=1 U11 switch is opened
with the U11 switch closed, the integrator sees the DAC voltage. This allows calibration of the integrator used for Cs calibration of the detector. With the switch open, the integrator sees only the phototube.

Set S1-S4   subadr=11101000 data=0000-s1-s2-s3-s4   s1=1 open switch U10-s1 etc.
                                                       s1=0 close switch U10-s1 etc
These 4 switches control the gain of the slow integrator. See integrator calibration software for the 6 meaningful values for the T-network opamp circuit.

Set MSE subadr=11101100 data=0000000x   x=0   MSE bit not set
                                                       x=1 sets the MSE bit on the selected 3in1 card.
A card is selected with Set TUBE and its MSE bit is set, then when MULTI_SEL is high, the card will respond to commands even with its card_sel line in not high. This allows a "broadcast mode" execution of commands to any subset of 3in1 cards.

ENABLE Small C subadr=11110000 data=0000000x   x=0 disable
                                                       x=1 enable
controls transmission of TP signals to the Small Capacitor (CS) for charge injection.

ENABLE Large C subadr 11110100 data = 0000000x   x=0 disable
                                                       x=1 enable
controls transmission of TP signals to the Large Capacitor (CL) for charge injection.

Set DAC subadr=111110xx data=xxxxxxxx
  sets the DAC on the selected 3in1 card.
       Volts = 4.096*DAC/1023 to integrator
       Volts=2*4.096*DAC/1023 to CL and/or CS

ENABLE TRIGGER OUTPUT subadr=11111100 data=0000000x   x=0 disable trigger output
                                                       x=1 enable trigger output
allows removal of selected 3in1 card from the trigger sum