THE ATLAS TILE CALORIMETER DIGITIZER

S. Berglund, C. Bohm, S-O. Holmgren, K. Jon-And, J. Klereborn, B. Selldén, S. Silverstein and J. Sjölin
Stockholm University
K. Anderson, J. Pilcher, H. Sanders and F. Tang
University of Chicago

Abstract

A prototype digitizing system for the Atlas Tile Calorimeter was developed for evaluation in the ATLAS test beam with the barrel preproduction module during the summer of 1998. The experiences provided important input for the final design, which must be ready for production during 1999.

The digitizer demonstrator consists of 8 boards for read-out of up to 48 channels, which are located in a TileCal "super drawer". The boards are connected in a chain ending in a Fibre-channel S-link interface which transports data at a rate of up to 132 MB/s to a Read Out Driver outside the detector. Each board handles the signals from the front-end electronics of 6 PMT channels. To achieve an overall dynamic range of 16 bits, a high and low gain output from each channel is digitized with 10 bit resolution. A XILINX FPGA controller extracts data from pipeline memories and formats the data for read-out. Commands for control and setup of the digitizer system are provided via a TTC system. An ACTEL PGA with fault tolerant design is used as a Read Out Controller.

1. INTRODUCTION

The Atlas hadron Tile Calorimeter [1] consists of 4 segments, each containing 64 wedge-shaped modules (fig.1). The two center segments form the barrel part and the others the extended barrel. The modules, in turn, consist of interleaved iron and scintillator tiles. Impinging particles produce showers in the iron tiles that cause light flashes in the scintillators.

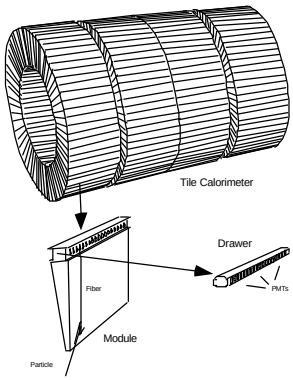

Fig 1. Schematic diagram of the Tile Calorimeter.

Light from the scintillators is transferred via wavelength shifting fibers to photomultipliers (PMT) in the base of the module. The PMTs and all other electronics are mounted on a sliding “drawer“, which can be removed from the module in one operation.

When excited by light the PMT produces a pulse which is shaped and amplified in a so-called 3-in-1 board [2] (fig.2). The pulses are amplified by both high and low gain channels, with a gain ratio of 64. Differential outputs from both amplifiers are then transferred to the digitizer.

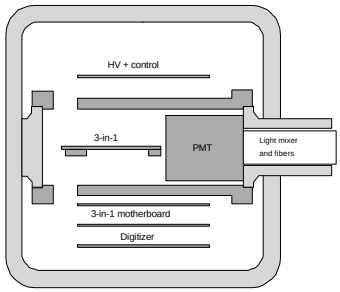

Fig 2 Cross section of the drawer and its case

2. THE DIGITIZER ARCHITECTURE

The size of the barrel drawers is 2.8 meters, along which 45 PMTs are mounted. The extended barrel drawers have the same size but contain only 32 PMTs. For practical purposes the digitizer is split up in boards of the size, 35x10 cm^2. The barrel digitizer consists of 8 such boards, while 6 boards are sufficient to serve the extended barrel.

The incoming pulses, high gain and low gain, are digitized every 25 ns by 10-bit ADCs. The data are stored temporarily in pipeline memories (fig.3) to await a level-1 trigger decision. The trigger latency is now slightly more than 2 μs. A sequence of samples is transferred to derandomizer buffers when a level 1 accept is issued by the first level trigger. In this way all pulses corresponding to the triggered event will be multiply sampled, allowing a subsequent detailed analysis to extract the correct amplitude value eliminating, as far as possible, contributions from later

pulses (pile-up). However, the buffer contents must be examined to make sure that an overflow did not occur in the high gain channel. In the normal read-out mode an overflow would cause read out of the low gain, rather than the high gain channel.

An event may contain up to 15 samples. Digital data from 3 inputs are packed together as 32 bit words to be transferred to a FIFO. There is also a controller part which is responsible for the insertion of control words into the data stream.

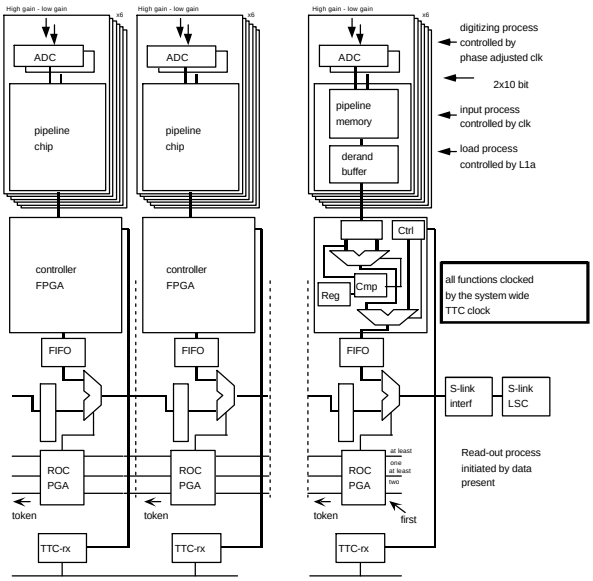

Fig 3 Schematic description of the TileCal digitization system

The FIFOs allows decoupling of the data insertion process (initiated by level 1 accept) and the readout which is connected with the FIFOs not being empty. If data is present in the FIFOs of at least two boards a read-out process is initiated by the first board. This procedure is adopted to increase the fault tolerance of the readout functions, since an error here would block readout of the preceding boards as well. Just before completion of its readout, the first board sends a token to the second board to start its readout in time so that its data can be appended to the stream. This process is repeated until the last board is read out. After this the first board again checks for new data in the FIFOs. The entire readout protocol is implemented in the Read-Out Controller (ROC).

The data from the digitizer boards are sent via a specially designed interface to an S-link fiber channel Link Source Card (LSC). The LSC sends the information via fiber to an S-link receiver Link Destination Card (LDC) in the ROD. The S-link protocol [3, 4] allows specially flagged S-link control words, which are used by the digitizer link layer. The ROC in the first board is responsible for inserting these extra control words.

The TTC system is used for clock generation, to deliver level one accepts, and for control and setup of the digitizer operation. Its phase-adjustable clock is used for the ADCs so that the incoming pulses can be sampled in corresponding positions. The TTC optical signal is converted to an electrical signal on the S-link interface board and then transferred with PECL logic levels to the individual boards where a TTC-rx ASIC interprets the protocol.

In the digitizer demonstrator the pipeline memory and the derandomizers are merged in TEC_DMU pipeline chips [5], which were originally developed for the PHENIX detector at RHIC. These chips contain a pipeline of programmable length and 5 derandomizer stages to store events selected by the first level trigger until they can be read out. The length of the pipeline and the derandomizer depth (192 and 80, respectively) are somewhat large for the TileCal application, but this does not have any serious consequences for performance.

A XILINX FPGA (XC4013XL) controller contains the high-gain/low-gain selection mechanism, as well as most control functions. Data from this controller is, as previously mentioned, stored in a synchronous FIFO before being sent out via a ROC controller to the next board and eventually to the S-link board. The FIFO was inserted since the number of derandomizers did not allow the necessary safety margin against data overrun. To enhance the reliability of the system the vital ROC was implemented in a A1225XL fusible link PGA from ACTEL. Such components have a certain degree of radiation tolerance which may be sufficient for the digitizer design. This must be validated by realistic radiation tests.

Both controller and read-out controller were designed from synthesized VHDL code.

3 BOARD DESIGN

One of the crucial issues when designing the digitizer board was to reduce the noise contribution before digitization to a minimum. This was achieved by using differential inputs, and careful design and layout of the circuit board. Analog and digital power and ground are well separated (fig.4) and connected only at one point. The layout of the channel related circuits was done interactively in two trace layers and then copied five times (see also fig.3). The remaining digital part, on the other hand, was autorouted into four trace layers. An 8 layer board was used for the fabrication. To avoid timing problems all signals that pass through several boards are resynchronized in each board.

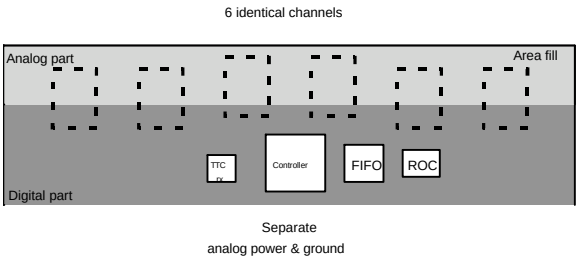

Fig 4 Board layout overview

4 COMMANDS AND DATA FORMATS

The digitizer is controlled by broadcast or addressed commands via the TTC B channel. The commands are interpreted in the controller. One can set the operation mode:

Normal mode: readout of either low gain or high gain data

Calibration mode: readout of both gains

Test mode: exercise the TEC_DMU test mode

It is possible to adjust the pipeline length (1 to 192), the number of samples in the derandomizers (5 to 15) and the timing of the ADC clocks. One may also set a 24-bit word that will be stored in the TEC_DMU during test mode and read back via the controller.

The two broadcast user defined bits produce a trigger when the system is in test mode. They can also reset the digitizer or the S-link or they can be used to force the S-link itself into test mode.

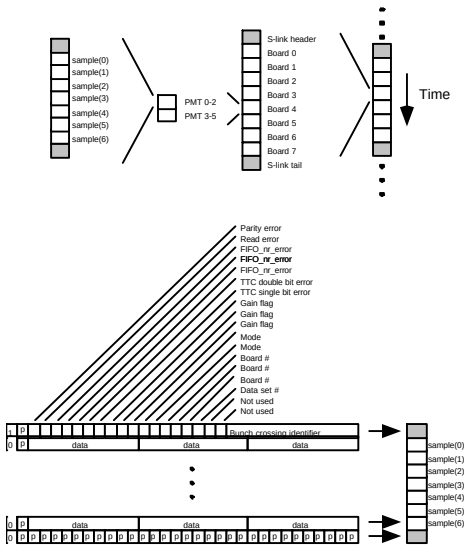

Fig 5 Data format during normal mode read-out.

In both normal (fig.5) and calibration modes, the data is read out event-by-event and board-by-board, with channels grouped three-by-three. All words are protected by parity, and an extra tail word provids vertical parity as well.

The header contains flags to identify the data, such as a bunch crossing identifier and board id. It also contains information about the gain setting for each ADC value and about the operation mode. Error flags monitor the digitizer operation and the TTC transmission. Single and double bit TTC errors are recorded.

5 TEST BEAM EVALUATION

After extensive tests in Stockholm with a chain of up to 8 boards and using internal stimuli and static external stimuli, the system was moved to a test bench at CERN where a small number of 3-in-1 boards provided dynamic stimuli. Five boards were installed in the barrel module 0 at the test beam (fig.6), towards the end of the test beam period. Data were then taken over 24 hours with pion, electron and muon beams.

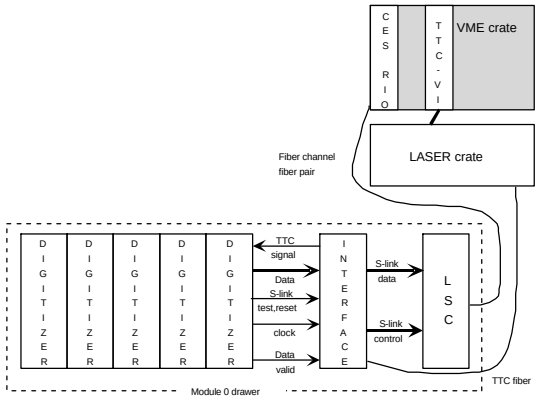

Fig 6 Test beam setup.

Almost full functionality was achieved. Preliminary analysis of test beam data (fig.7) shows a noise level of 1.1 LSB (~17 MeV) for the high gain channel, which agrees well with SPICE simulations of the 3-in-1 boards. The low gain channels give a noise level of 0.5 LSB (~0.5 GeV).

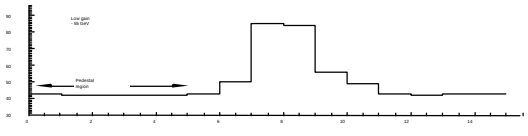

Fig 7 A sample pulse.

6 NEXT VERSION

The final design must be radiation tolerant [6] up to 100 Gy over 10 years of operation, which influences the design and choice of components. For instance, the XILINX FPGA must be replaced. It is also necessary to find a radiation tolerant version of the S-link. A modified TEC_DMU is being planned which will help simplify the design, as well as reduce the cost and increase radiation tolerance.

The new TILE_DMU should contain additional registers and comparators for gain comparisons. By allowing the gain selection decision to be made by the TILE_DMU, a smaller and less complicated controller design can be used, since it is no longer in the data path.

Additional design improvements for the TILE_DMU include:

- Improved test facilities, e.g. JTAG.
- A 12-bit data path instead of 24 bits will allow a smaller package.
- More derandomizers (8 instead of 5) will eliminate the need for an extra FIFO
- Smaller feature size such as 0.35 µ instead of 1µ process provides reduced chip size increased radiation tolerance and faster logic, allowing safer design (that can be synthesized)
- 3.3 V instead of 5V operation

The new TILE_DMU will also reduce the board complexity and will lead to an improved reliability. It is also possible to introduce a modularity that allows 6, 9 or 12 channel boards.

7 SUMMARY AND CONCLUSIONS

Based on ideas and experience from the RD-16 (FERMI) project [7], a digitizer has been designed for the Tile calorimeter. A fully functional prototype for the TileCal Digitizer was developed and tested in the test beam summer 1998 with encouraging results. The additional noise contribution of the new digitizer proved to be small.

A final version of the digitizer is currently being designed (and subjected to mandatory design reviews) to be verified in the 1999 test beam, and installed in the first production TileCal modules towards the end of 1999. A new pipeline chip is being developed to bring down system cost and to achieve sufficient radiation tolerance.

8 ACKNOWLEDGMENTS

Many persons were involved in the design and tests of the digitizer. Pontus Stenström and Lars Thollander from Stockholm University gave valuable help in the board layout and the design of the S-link interface. Alfonso Rios from University of Valencia wrote the DAQ software and the TileCal test beam crew helped to run the the system.

The digitizer design relied on the TTC hardware for timing and transfer of commands, and S-link boards for extraction of data. The help from both support organizations are gratefully acknowledged. We were early users of both systems. Erik van der Bij gave us valuable advice and reviewed the design of the S-link interface board.

9 REFERENCES

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