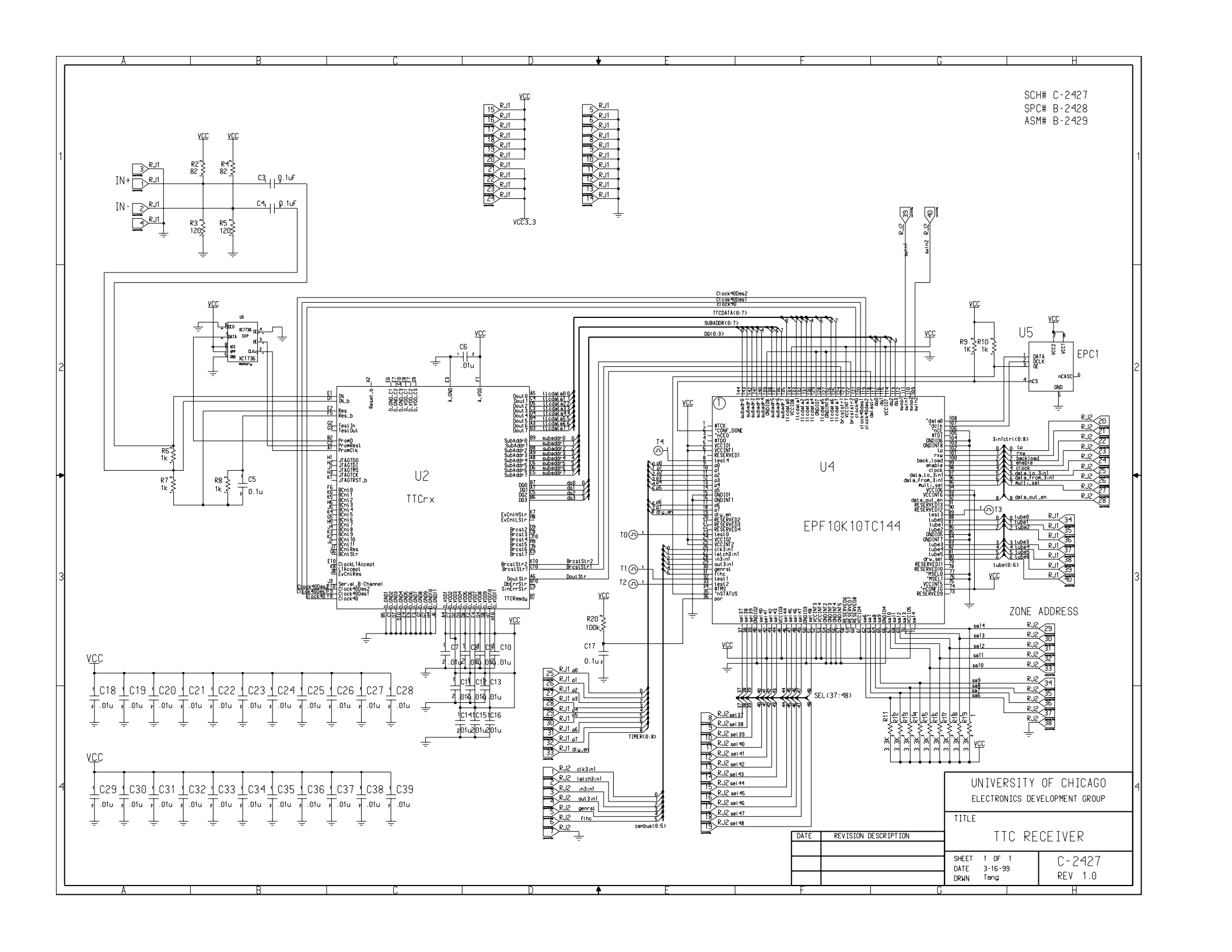
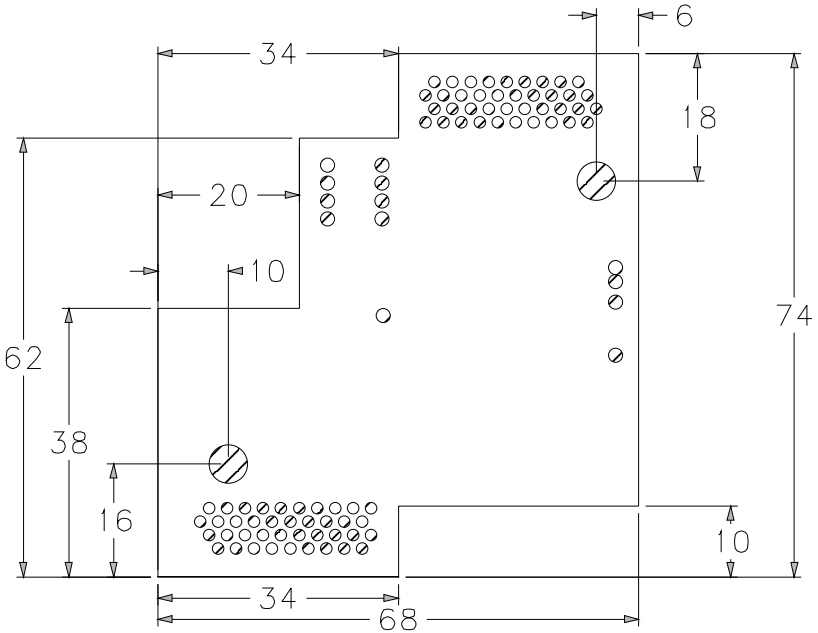

SCH# C-2427
SPC# B-2428
ASM# B-2429
U2
TTCrx
U4
EPF10K10TC144
U5
EPC1
ZONE ADDRESS
SEL(37:48)
TIMER(0:8)
canbus(0:5)
tube(0:6)
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP
TITLE
TTC RECEIVER
DATE
REVISION DESCRIPTION
SHEET 1 OF 1
DATE 3-16-99
DRWN Tang
C-2427
REV 1.0

B2428 Specification Drawing



Mount Hole: m_200_dr_130 (mil)
Board Unit: mm

BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.015	262	YES	---
⊞	.035	80	YES	---
⊕	.041	13	YES	---
⊟	.13	2	YES	---

B2367 PC BOARD SPECIFICATIONS

1. Board Layers: 6

2. Layer Stack Order:
   Layer1 (Film1): Top component layer(signal_1).
   Layer2 (Film2): Power plane(Power,VCC).
   Layer3 (Film3): Power plane(Power,V3_3).
   Layer4 (Film4): Inner signal layer(inner, signal_3).
   Layer5 (Film5): Ground plane (Power,Ground).
   Layer6 (Film6): Bottom component layer(signal_2).

3. Apply solder mask over bare copper on both side:
   Film7: Top component side solder mask.
   Film8: Bottom component side solder mask.

4. Apply silkscreen on both side:
   Film9: Top component side silkscreen.
   Film10: Bottom component side silkscreen.

5. Material: FR4.
6. Board thickness: 0.062'' +/- 0.010.
7. All layers are equal thickness.
8. Copper thickness 1oz before plating.
9. All dimensions are in inches unless otherwise noted.

10: Contact person:

Fukun Tang/Electronics Engineer
Electronics Development Group
University of Chicago
Tel: (773)-702-7801, Fax: (773)-702-2971

SCHM# 2447
SPEC# 2448
ASSM# 2449

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
B2448 Specification Drawing

SHEET 1 OF 1
DATE 3/24/99
DRAWN TANG

B- 2448
REV 1.0