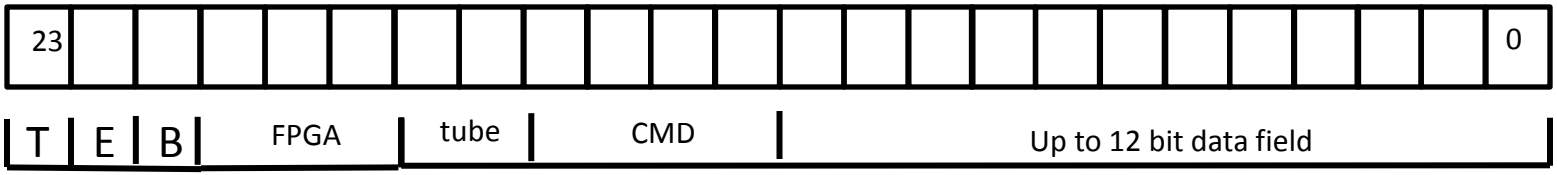
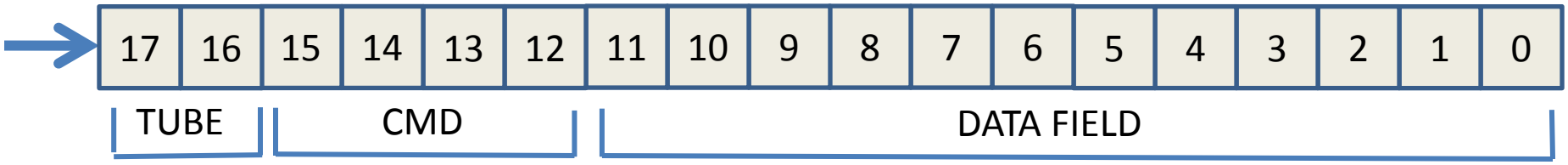
24 bit command sent to mainboard FPGA's



T – charge injection timing phase control & adc control
E – daughter board to transmit command to mainboard
B – daughter board to retrieve 12 bits from mainboard
FPGA – which mainboard FPGA should execute the command
- 000 – FPGA A0
- 001 – FPGA A1
- 010 – FPGA B0
- 011 – FPGA B1
- 1XX – all FPGAs

Tube – which 3in1 card associated with the FPGA to execute the command
- 00 – 3in1 card far from patch panel
- 01 – center 3in1 card
- 10 – 3in1 nearest patch panel
- 11 – all 3 3in1 cards



CMD – 0000 set 3in1 switch values
0001 set 3in1 DACs
0010 set readback shift register with 3in1 settings
0011 set readback shift register with 3in1 DAC setting

After sending these commands the daughterboard waits for execution and then clocks back the data

0100 set ADC offset High Gain plus DAC
0101 set ADC offset High Gain minus DAC
0110 set ADC offset Low Gain plus DAC
0111 set ADC offset Low Gain minus DAC

Registers in FPGAs

1000 set readback ADC offset High Gain plus DAC
1001 set readback ADC offset High Gain minus DAC
1010 set readback ADC offset Low Gain plus DAC
1011 set readback ADC offset Low Gain minus DAC

After sending these commands the daughterboard waits for execution and then clocks back the data

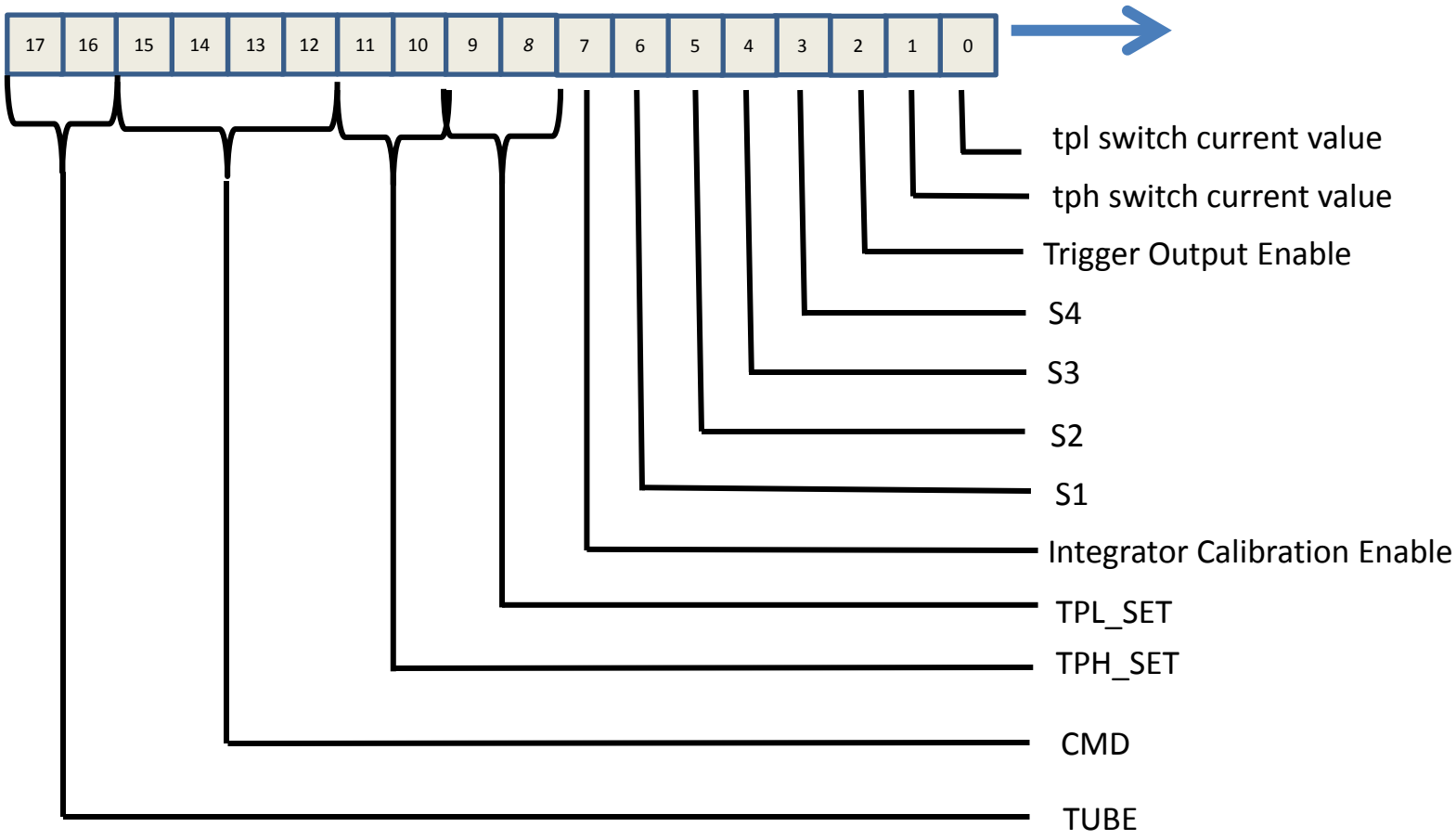
1100 load ADC DAC high gain of specified tube (no data field)
1101 load ADC DAC low gain of specified tube (no data field)

Transmits Register Pair to DACs

1111 global reset

DATA Field
for command=0000
11-10 TPH - small capacitor charge injection control bits
10= open switch to charge small capacitor
01=close switch (inject charge on capacitor)
00=pass through injection signal from DaughterBoard
9-8 TPL - large capacitor charge injection control bits
10= open switch to charge small capacitor
01=close switch (inject charge on capacitor)
00=pass through injection signal from DaughterBoard
7 Integrator Calibration Enable
6-3 integrator gain switches S1-S2-S3-S4
2 Trigger Enable
1-0 unused
for DAC set commands
11-0 appropriate 12BIT DAC latched value

READBACK Word (18 bits)

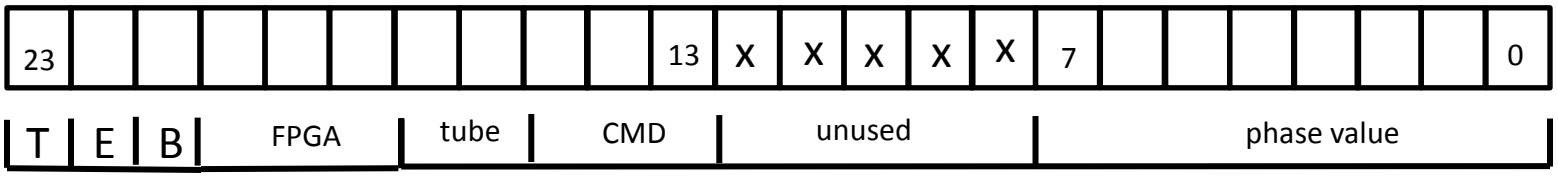


OR

11 downto 0 = 12bit appropriate DAC latched value

CIS timing phase

24 bit command sent to mainboard FPGA's



Reset Phase Control

Set T=1, E=0,FPGA,TUBE,CMD=0

Set Phase for a particular tube

Set T=1, E=0,FPGA,TUBE,CMD=1 data field[5 downto 0] = phase value

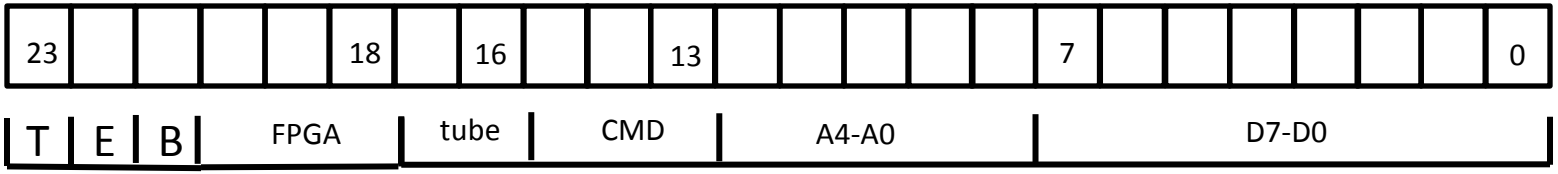
Readback Phase (followed by a B=1 command)

Set T=1, E=0,FPGA,TUBE,CMD=2

Note: T=1 commands have a 3 bit CMD field

ADC Control

24 bit command sent to mainboard FPGA's



Set ADC mode

Set T=1, E=0,FPGA,TUBE,CMD=3 d0=0 (serial) d0=1 (parallel)

parallel is the power on default

Set ADC control register

Set T=1, E=0,FPGA,TUBE,CMD=4

address=data field[11..8]

data=data field[7..0]

Readback ADC register to ADCBACK register

Set T=1, E=0,FPGA,TUBE,CMD=5

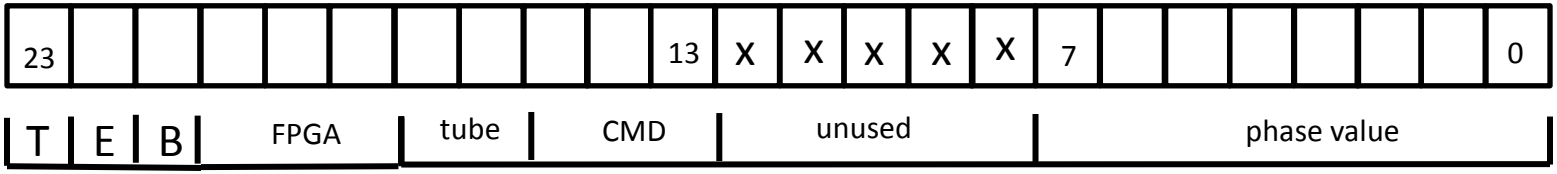
address=data field[11..8]

Readback ADCBACK register

Set T=1, E=0,FPGA,TUBE,CMD=6 (follow with a B=1 command)

Note: T=1 commands for the ADCs have a 3 bit CMD field

24 bit command sent to mainboard FPGA's



B=1, FPGA=0,1,2, or 3
Daughter board retrieves data from designated FPGA output register.