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Mezzanine card specifications for Level-2 Calorimeter Trigger Upgrade

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Abstract

We describe here the design specifications for the mezzanine card used by the Level 2 Calorimeter upgrade. This card will receive calorimeter trigger tower energy from DIRAC at full resolution and send it to a PULSAR board through onboard connectors. It needs to receive the LVDS signals from four input cables and transform it to TTL for processing by an onboard FPGA. The FPGA will serialize the data and append two bits with location information. It will be programmable through a JTAG connector. The operations will be conducted synchronous to an onboard clock running at 4 times the CDF clock frequency (33 ns).

1 Overview of L2CAL upgrade hardware configuration

At the hardware level, the L2CAL upgrade is to use Pulsar boards to receive the raw (full 10-bit resolution) trigger tower energy information from the DIRAC boards (L1CAL Trigger), merge and convert the data into SLINK format, then deliver the SLINK package to the L2 decision PC. This is very similar to what has been done to all the other L2 trigger data paths for the L2 decision Pulsar upgrade. In that sense, this can be viewed as a natural expansion of the L2 decision upgrade. In fact, since the clustering algorithm would now be done in software inside the L2 decision CPU, the proposed L2CAL system will be much simpler and much more uniform at the hardware (and firmware) level.

For the existing L2CAL system, since the actual clustering (also isolation) is done in hardware (designed in the mid 90's), the system is quite complicated. The entire system consists of 86 9U VME boards in 6 VME crates with a custom P3 backplane, including 72 DCAS, 6 LOCOS, 1 CLIQUE, 6 IsoPick and 1 Iso-Clique boards.
The proposed L2CAL upgrade system will consist of 18 Pulsar receiver boards, and 6 existing Pulsar SLINK merger boards (See figure 1). Since the Pulsar receiver only needs to receive the raw data and convert it into SLINK format, the firmware for the Pulsar receiver board will be simple.
In order to receive the trigger tower energy (LVDS signals) from the DIRAC boards, a new Pulsar mezzanine card will need to be designed. One mezzanine card should be able to receive 4 cables from DIRAC (corresponds to one DCAS input data), thus one Pulsar board can receive 16 cables or 4 DCAS input data.

Figure 2 shows the existing hardware involved in the upgrade, with the red part being the new L2CAL path. In particular the new path take as input the raw trigger tower energy information from DIRAC board (LVDS signals) and deliver them directly to the L2 decision CPU (SLINK format). The new Pulsar crate receives as inputs the same information that DCAS receives in the running system.
To minimize the impact on the running system, i.e. to be able to run in pure parasitic mode during commissioning, we will make a copy of the LVDS input signals. In this case, we will use the LVDS "multi-drop" property, and make long cables in such a way that each DIRAC output signal LVDS cable first has a "drop" at a Pulsar mezzanine card (without termination during commissioning), then goes to the existing DCAS input (which has 100 ohm termination). See Fig. 4.
In other words, the signal splitting is simply being done with long cables having one additional connector. In Fig. 3 the basic idea (not detailed) of the new cabling is reported.

In the current system, one DCAS board receives four input cables. In the new system, one Pulsar mezzanine card will receive the same amount of input data as one DCAS. Figure 5 shows the mezzanine card design. Note that the length of the mezzanine card will be doubled, with respect the length of the standard Pulsar mezzanine, to allow easy access to all four LVDS cables. With four mezzanine cards per Pulsar board, 18 Pulsars (in two crates, see Fig 1) will be needed to receive all input data.

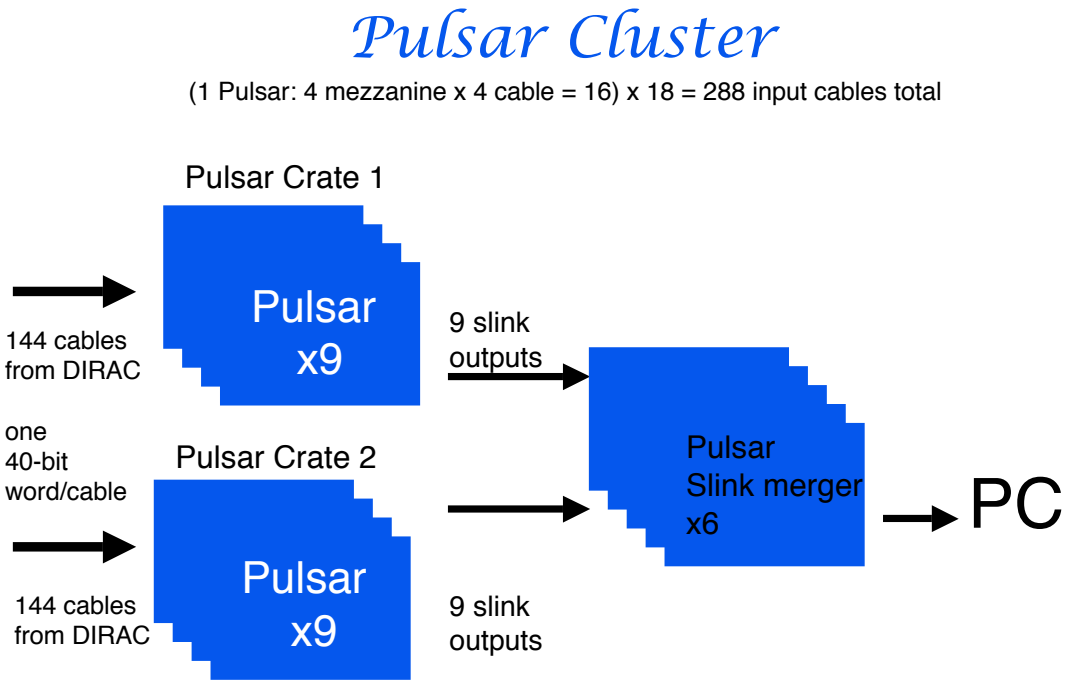

Figure 1: L2CAL upgrade: 24 Pulsars merge data from the DIRAC cards directly into the Level 2 decision PC. The system includes 18 Pulsar receiver boards and 6 Pulsar SLINK merger boards (already used and tested).

The rest of the system consists of existing Pulsar SLINK mergers

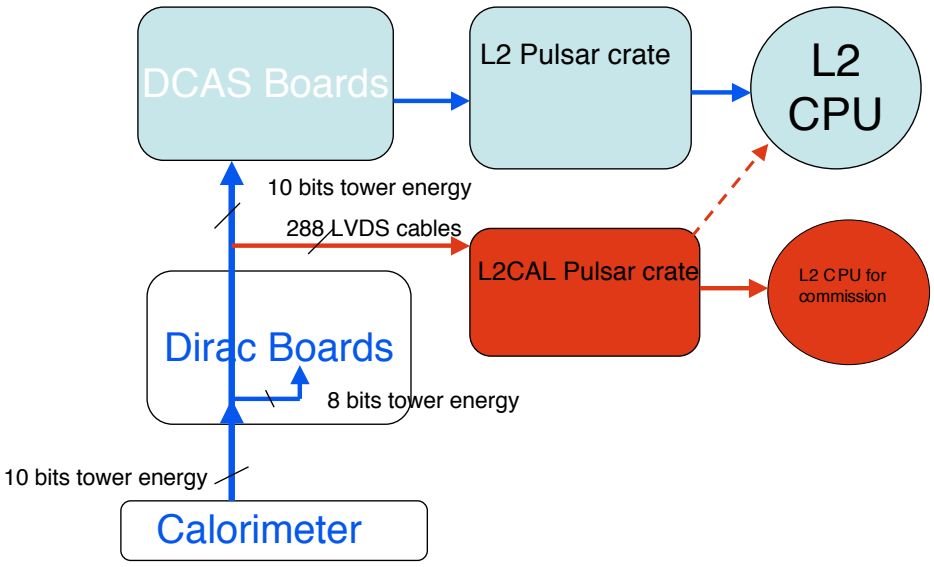

Figure 2: The red path represents the new hardware to be added to the calorimetric trigger system.

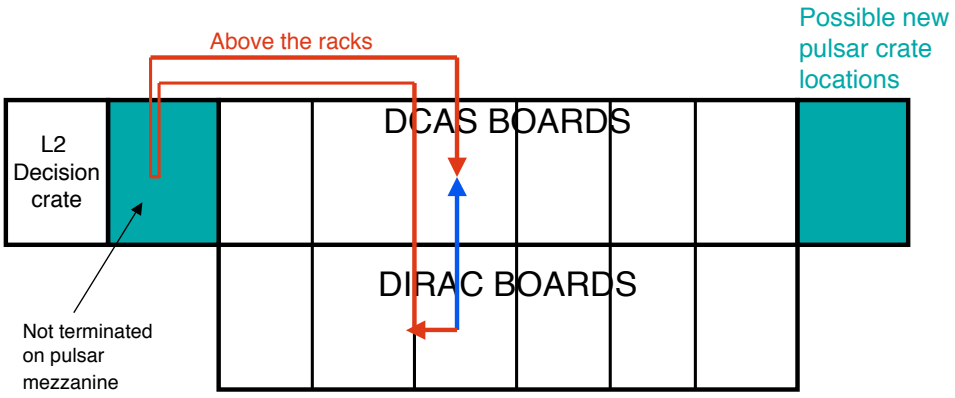

Figure 3: The red new Pulsar crate (green) and the basic idea (not detailed) of the new cabling (red).

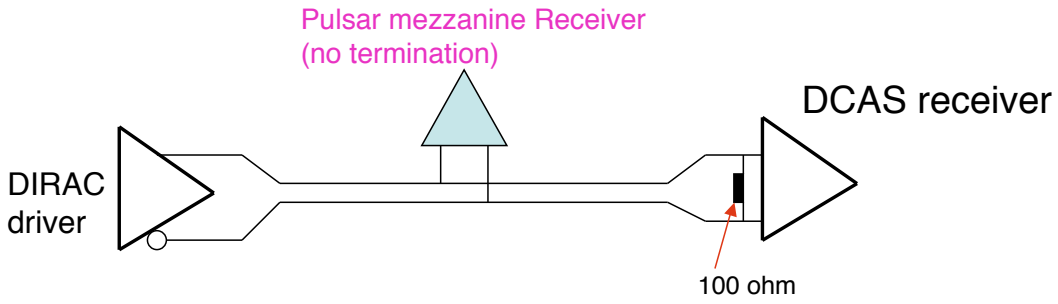

Figure 4: The bypass on the data path to operate the new and old systems together. A copy of the LVDS signal caming from DIRAC boards and going to DCAS boards is made available to the new system (Pulsar receiver). This is made possible by using the mutidrop property of the LVDS signals. During commissioning we run the new system in pure parassitic mode (i.e. without termination on new Pulsar Mezzanine receiver). As soon as we are ready to operate the change from the old to the new system, we add the termination on the new Mezzanine.

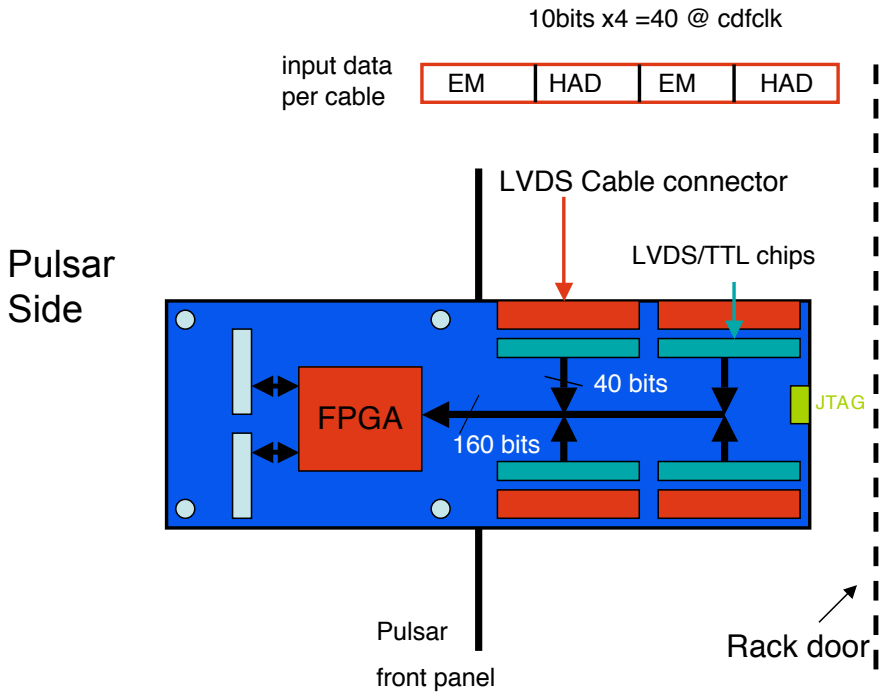

Figure 5: A simplified top view of the mezzanine card.

2 Pulsar receiver design overview

The Pulsar Cluster receives LVDS signals (288 cables), processes data and merge them into a single SLINK cable connected to the L2CPU.

The SLINK merger pulsars (see fig 1) have been already developed and tested during the last L2 upgrade. So in the following we'll give an overview of the design of the 18 pulsars receiving the LVDS signals from DIRAC boards and converting data into SLINK format. The data flow through the pulsar is shown in figure 6.

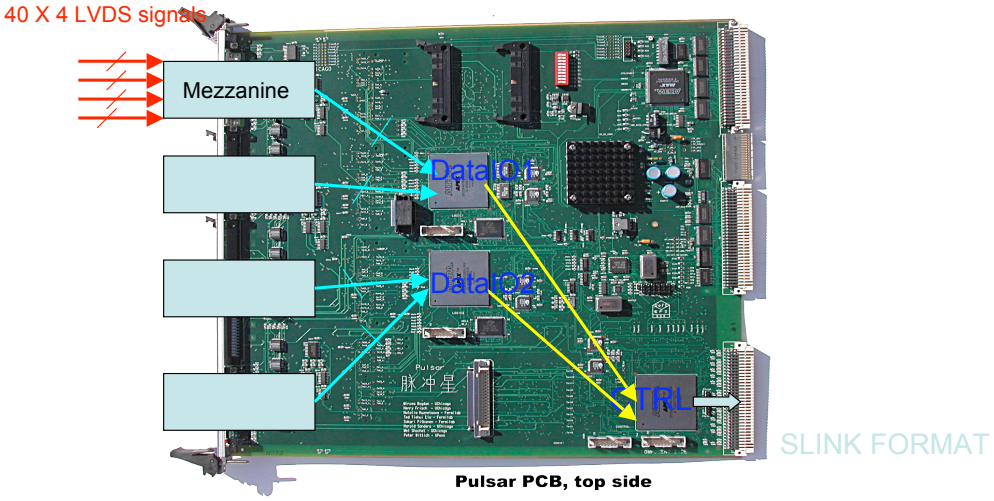

Figure 6: Data flow through the new Pulsar: 4 receiver Mezzanines receive 16 LVDS cables, then 3 programmable devices (2 IOs and 1 CTRL) process data, merge them and convert them into SLINK format.

The basic tasks of these new pulsars are:

1 Receive LVDS signals and convert into TTL. Each Board receives 16 LVDS cables (4 on each mezzanine), corresponding to 32 towers.

2 Select only the events confirmed by the L1A

3 Select only the towers with Non-zero Energy (Zero suppression)

4 Flag the tower energy information with the index of the sending tower.

5 Merge them into Slink format

The first item will be performed inside the mezzanine card. Items 2,3,4 will be performed inside the IO1 and IO2 FPGAs and the last one (merging the data) will be distributed in the 3 FPGAs along the data flow, starting on the mezzanine and ending on the CTRL FPGA. The firmware of the CTRL already exists, the only parts we have to take care are the LVDS receiver mezzanine design and the IO1-IO2 FPGA firmware.

3 Mezzanine Specification

The new mezzanine card has to perform the following tasks:

- Receive 160 LVDS signals @ CDF clock frequency (132 ns) and converts them to TTL signals. Each LVDS cable allows to transfer 2 tower energy information per word. At each CDF clock cycle we receive the information from 8 towers.
- Sends tower information to Pulsar adding 2 bits indicating the data arriving cable.

The data lines available on a single Mezzanine-Pulsar connector are 64. For each mezzanine we have 2 connectors for a total of 128 pins. 79 of them are available for signals. So the mezzanine can send only 2 tower information (40 bits) at once to the Pulsar. Because the mezzanine receives 8 tower information @ CDF clock frequency, we decided to send 2 tower information to Pulsar @ 4xCDF clock frequency.

3.1 Basic requirements and components

In picture 7 a the top-level diagram of the mezzanine is shown.

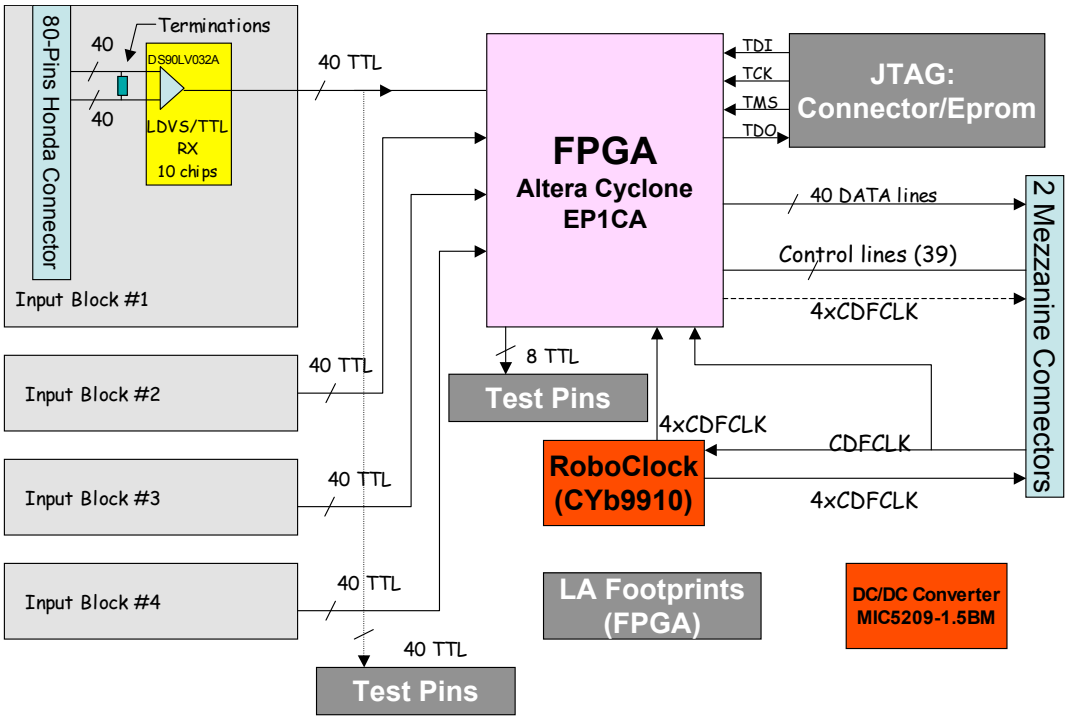

Figure 7: Top-level diagram of the Mezzanine.

4 logical input blocks receive the input data from the LVDS cables at CDF clock frequency. The 4 input blocks convert the LVDS signals into TTL signals and send them to the FPGA. The FPGA just merges the 160-bits input data into one 40-bit output data. The output will be sent to the Pulsar at 4x CDF clock frequency. The FPGA also adds 2 bits indicating the data arriving cable.

The mezzanine includes the following components:

- 4 LVDS cable connectors.
  They are 4 80-**pin Honda connectors**. Each connector receives 40 LVDS signals @ CDF clk frequency.
- 4 input blocks for LVDS to TTL translation.
  Each input block includes 10 **DS90LV032A** receiver chips.
  Terminations will be designed on the RX mezzanine near the RX chips, but they cannot be activated until we use the LVDS multidrop funtion. We are planning to place the footprint on the board with a leg already connected and the other to be connected later, so that the resistors can be soldered when the mezzanine is assembled, even if activated only at the end of the commissioning.
  The lines routed between the LVDS connector and the RX chips cannot be longer than 1.5 cm to be sure the LVDS multidrop function will work correctly.
  The power supply for chips is 3.3 V.
- Power Supply of the mezzanine is of 3.3 V
- 1 **Cyclone FPGA**. 3.3 V of power supply for the I/O and 1.5 V for the core.
- In order to generate the lower voltage for the core of the FPGA (1.5 V) we use 1.5V regulators (**MIC5209-1.5BM**)
- 1 Eprom to program FPGA
- JTAG Interface
- 2 set of Test pins: one for input signals (40) and one for signals coming from FPGA (8).
- 1 Roboclock to multiply the CDF clock frequency(**CYb9910**). The new clock should be also sent to the FPGA, where two internal PLLs can be used to adjust $4x$CDF clk.
- 2 Mezzanine-Pulsar Connectors. We have available 64X2 pins and 79 can be used as data/controls/clk signals (see next section for more details). All of them will be connected to the FPGA pins, even if theyll not be used, for possible future use.

3.1.1 Interface

In the following you can find a list of the RX mezzanine Inputs/Ouputs. See picture 8.

Input:

- 40X4 LVDS signals from the cables.

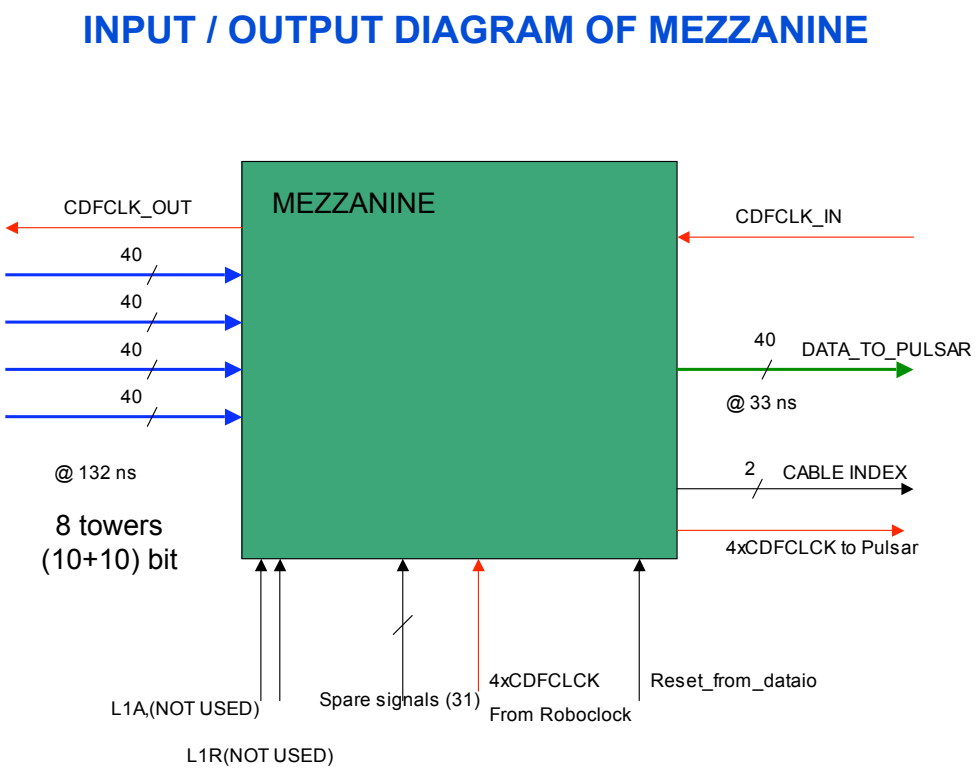

Figure 8: RX Mezzanine Inputs/Outputs.

- 4XCFD clk from Roboclock
- CDFCLK_IN CDF clock, for the input registers.
- RESET from Pulsar
- L1A* from Pulsar (NOT USED, just for future possible uses)
- L1R* from Pulsar (NOT USED, just for future possible uses)

Output:

- 40 TTLs signals to Pulsar
- 2 Controls Signal: cable connector index
- 4XCDK clk signal. This signal could be sent to Pulsar directly by the Roboclock, or, if necessary, after has been adjusted by the PLL inside the FPGA.
- CDFCLK_OUT Output of the PLL. CDFCLK_IN.

The available 79 pins on the mezzanine-pulsar connector will be used as follow:

- 40 for data bits

- 2 for control bits (cable connector index)
- 3 for clock lines (on dedicated ones): CDF clk, $4X$ CDF clk directly connected to the Roboclock, 4 CDF clk connected to the FPGA, after PLL.
- 1 for Reset signal from Pulsar to FPGA
- 2 for L1A and L1R

We have 31 spare control lines between FPGA mezzanine and motherboard.

3.2 FPGA Requirements and firmware

The firmware will be very simple: a description of the firmware implementation is given in figure 9.
The basic FPGA requirements are listed in the following:

- 250 pins available as data/control/clock pins: enough to handle 160 TTL (Cables Inputs) plus 40 TTL Output (to Pulsar) plus 39 control/clock signals to be connected to motherboard (total:239).
- Double power supply: 3.3 V for the and 1.5 for the core.
- PQFP Package.
- PLLs inside in order to adjust the CDF clk, if necessary.

We plan to use Altera Cyclone2 (EP2C15A).

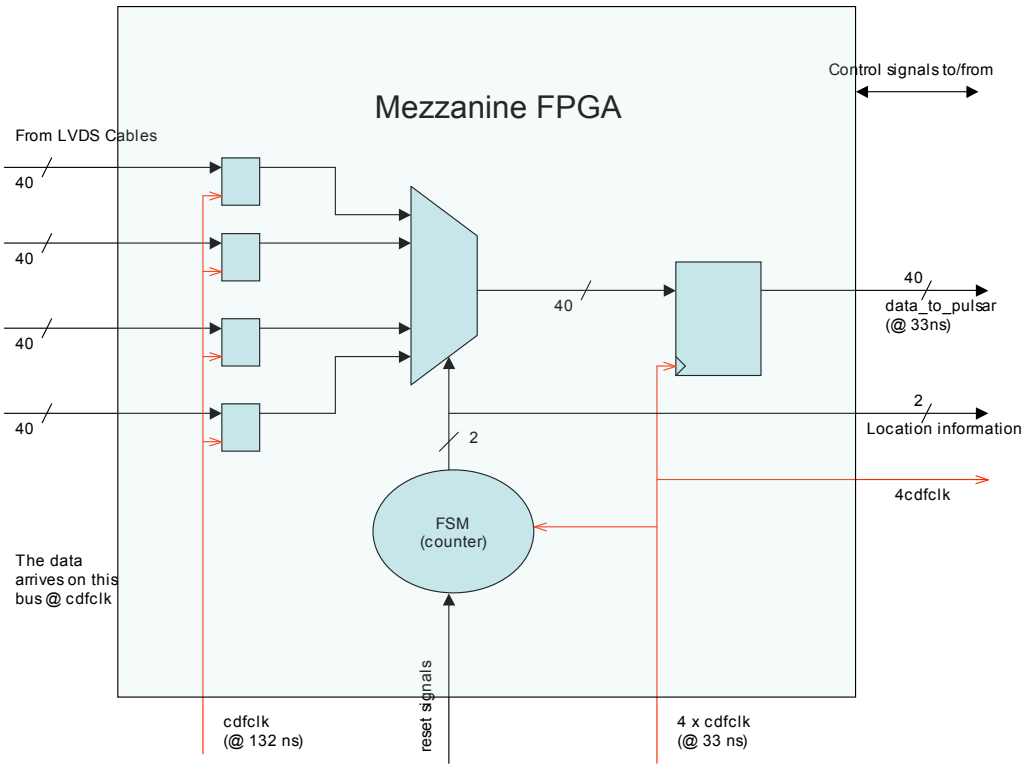

Figure 9: Mezzanine FPGA Logic. It includes 4 input registers and an output register with a MUX in the middle to merge the 4 inputs in a single output. The input registers work at the CFD clock frequency and the output register with a 33 ns clock (4 x CDF clock).

3.3 Test point

:

This is a set of Test Points suggested.

- 1 test point for each receiver chip. Each chip provides 4 data bits, we connect one of them to a test point placed right near the output of the chip (TTL side). In total we have 40 test point for incoming data. (see Fig 10)
- 1 test point for each of the following signals coming from the FPGA : L1A, BC (Beam Crossing), Reset, L1B1 and L1B2 (Buffer Bits) and one Spare, plus two signals coming from the Roboclock: CDF clk and $4X$ CDF clk. Total of 8 signals. We should be able to access these signals also when the we fully load the crate, so the test points should be placed on the outer part of the mezzanine.
- Just for testing pourpose we plan to have a Logical Analyzer connector for signals caming from the FPGA, placed on the inner part of the Mezzanine (inside the

Pulsar). The footpint of the connector is required.

- Vias on output signals (40 FPGA output to Pulsar plus few control signals between Pulsar and FPGA).
- Vias for each LVDS Cable Inputs (160 signals).

3.4 Mezzanine Layout

In figure 10, 11 and 12 the most promising design of the mezzanine layout is reported. The design shows the pulsar with 4 mezzanines with real sizes, both for connectors, cables and RX chips.

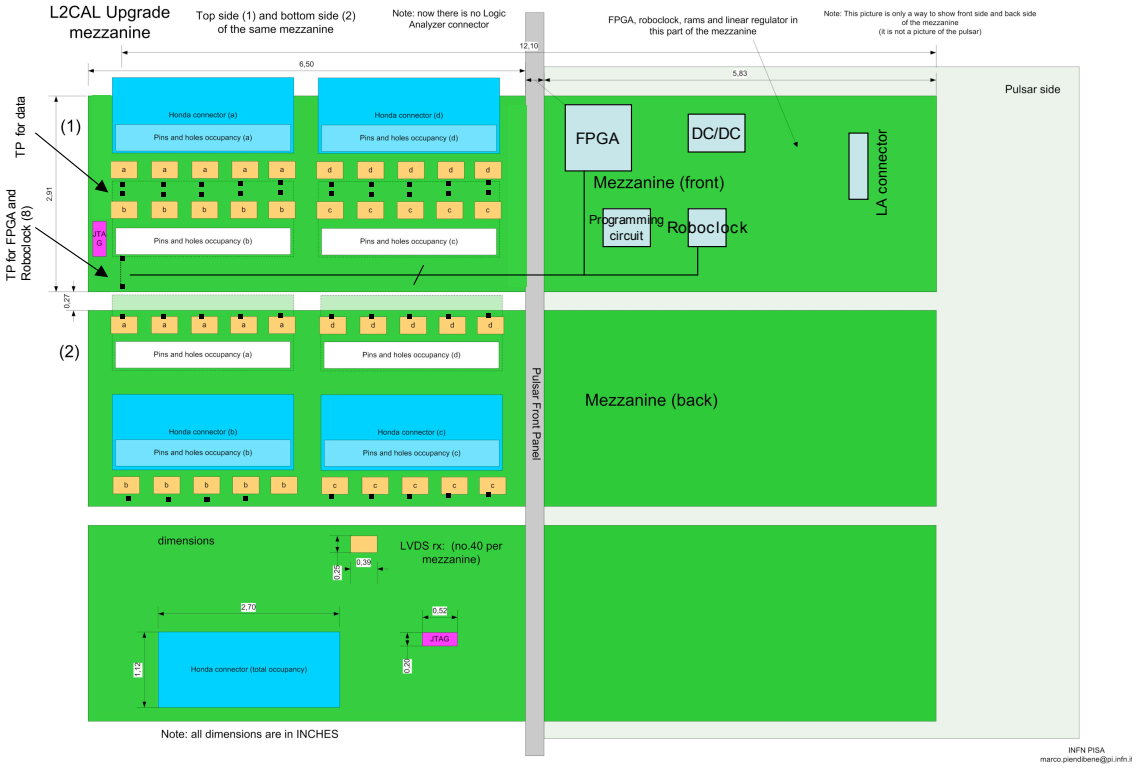

Figure 10: Mezzanine Layout.

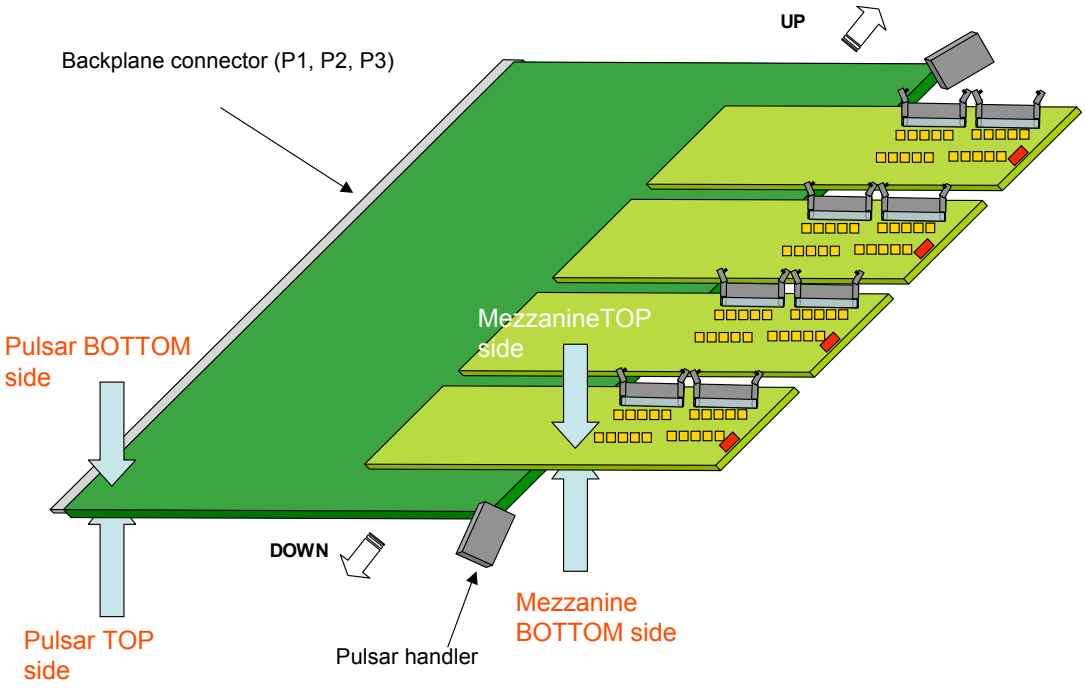

Figure 11: Mezzanine Layout: Top and Bottom face

3.5 Cabling

In figure 13 and 14 the details of the cabling are shown.

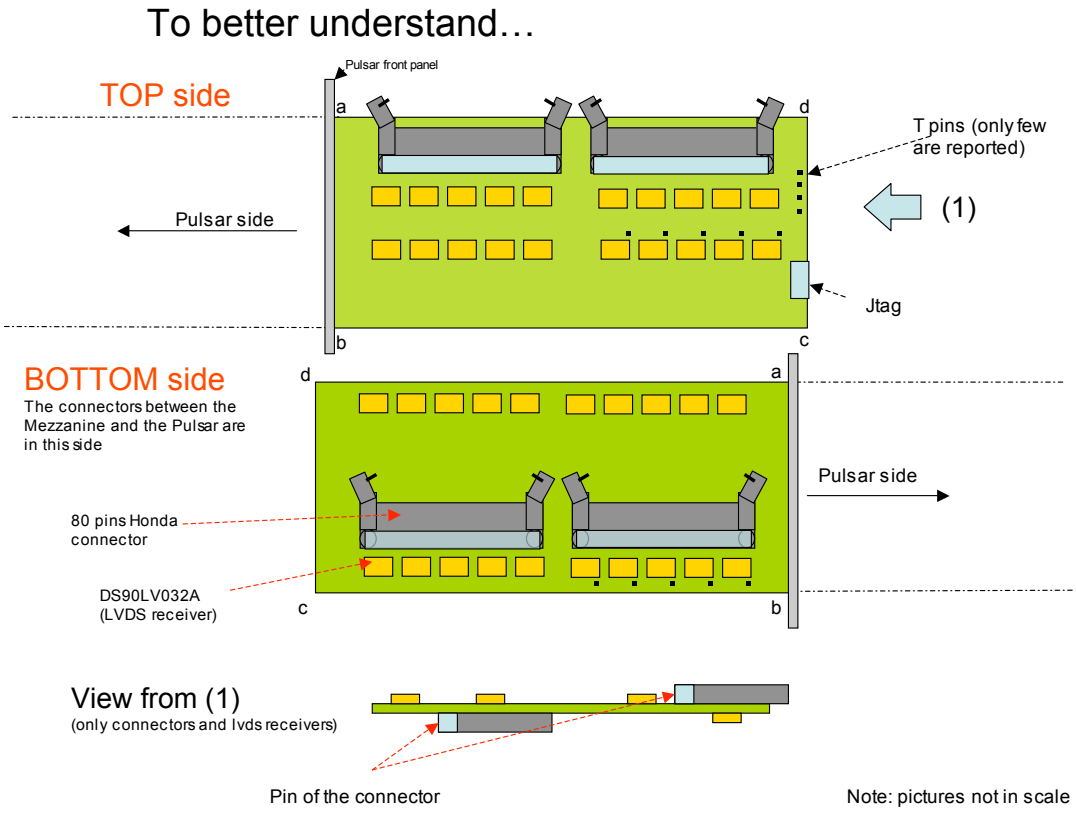

Figure 12: Mezzanine Layout: more details.

APPENDIX A:Transmitter and Receiver Mezzanine

For the upgrade we need a set of LVDS receiver mezzanine cards ($18x4+$ spares, we call them RX mezzanines), but for testing purpose we also need a set of LVDS transmitter mezzanine cards (4+ spares, we call them TX mezzanines). Probably, for space constraints, the best strategy will be the production of two separate boards, very closely related, one executing the RX function and the other the TX function. The difference between the TX and RX mezzanine will be really small. The main items concerning with the two boards are the following:

- For the RX board a set of LVDS/TTL converter chips is required (RX chip), while, for the TX board, we need a set of TTL/LVDS converter chips (TX chip). The RX and TX chips have the same sizes and very close pinout, but unfortunately they are not exactly pin-compatible.
- For both TX and RX board all the data/control lines are mono directional. In particular the signals changing direction from one board to another are the 160

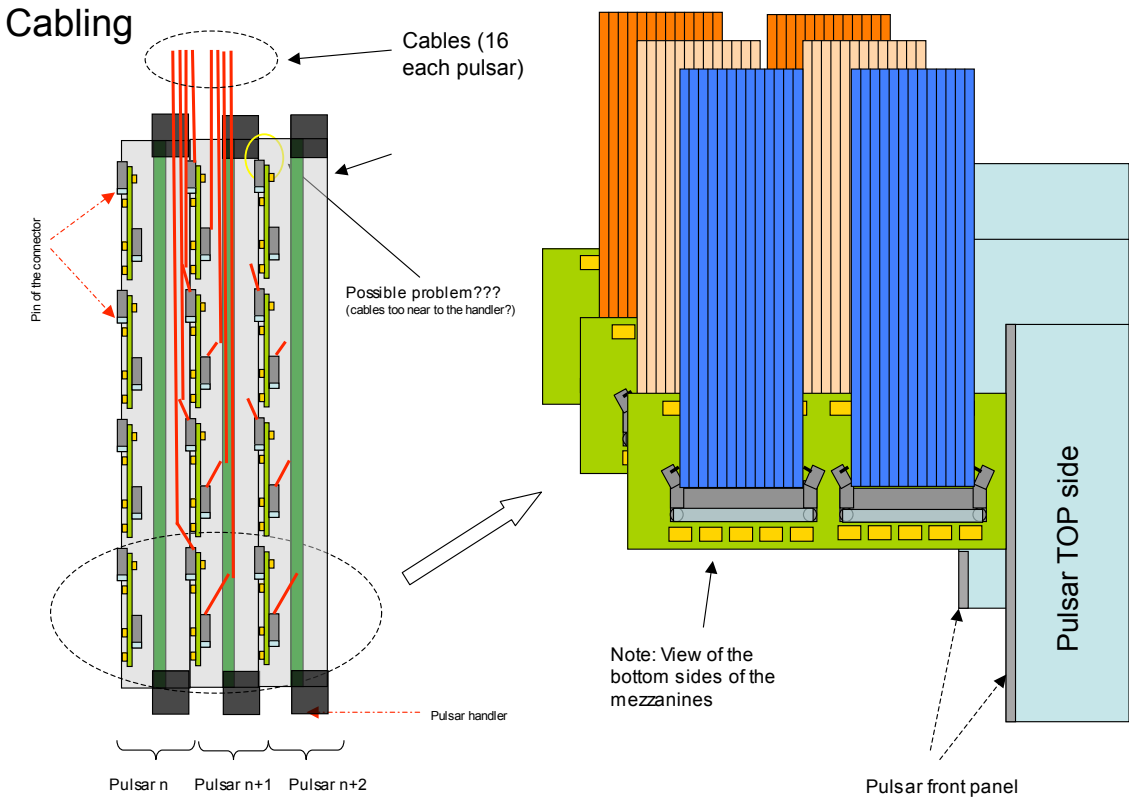

Figure 13: Cabling strategy.

lines to/from LVDS connectors and the 40 data from/to Pulsar. In addition we probably have few control data lines from/to Pulsar.

- The firmware inside the FPGA should be changed according with the board function. We can also think about the possibility to select the firmware according with a VME register.

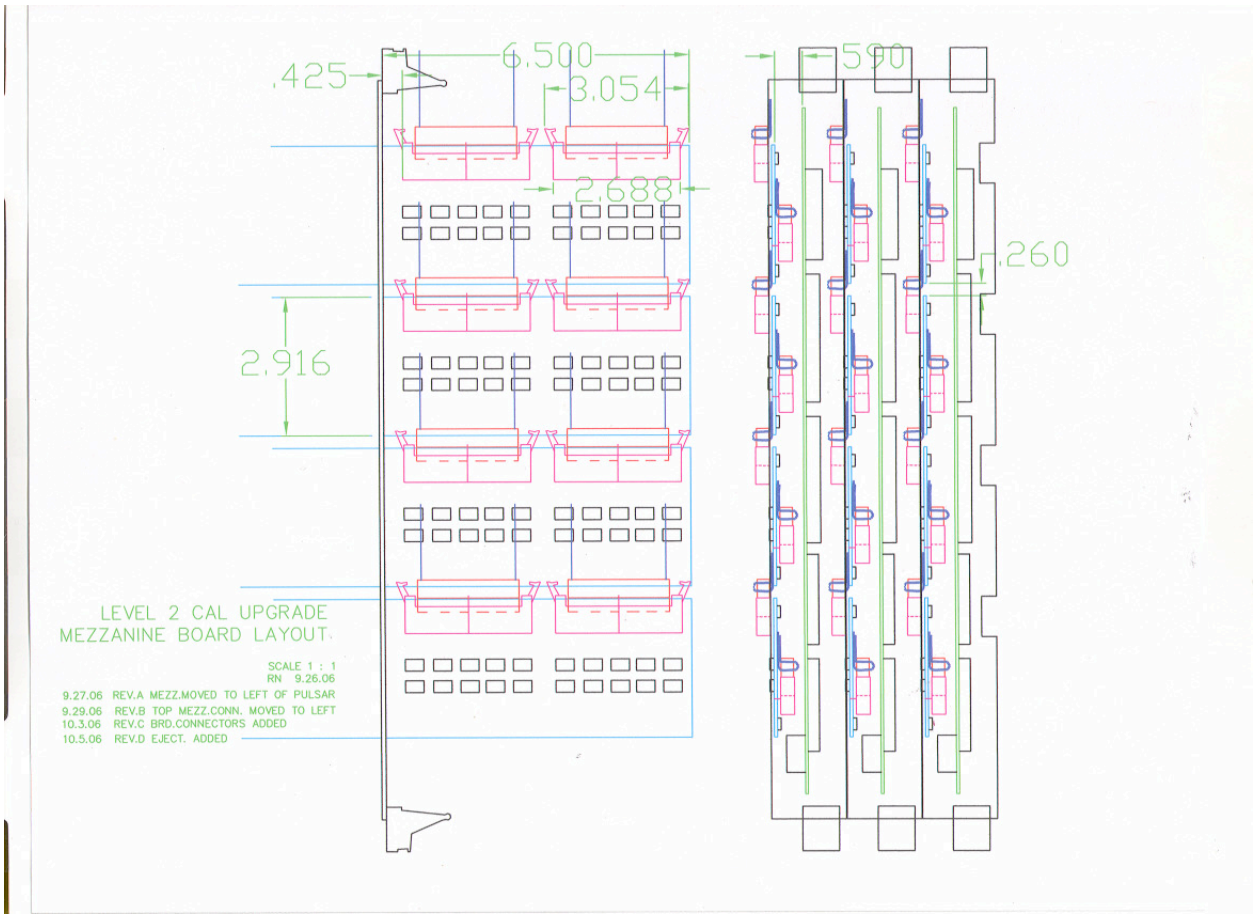

Figure 14: Cabling and Layout of the Mezzanine.