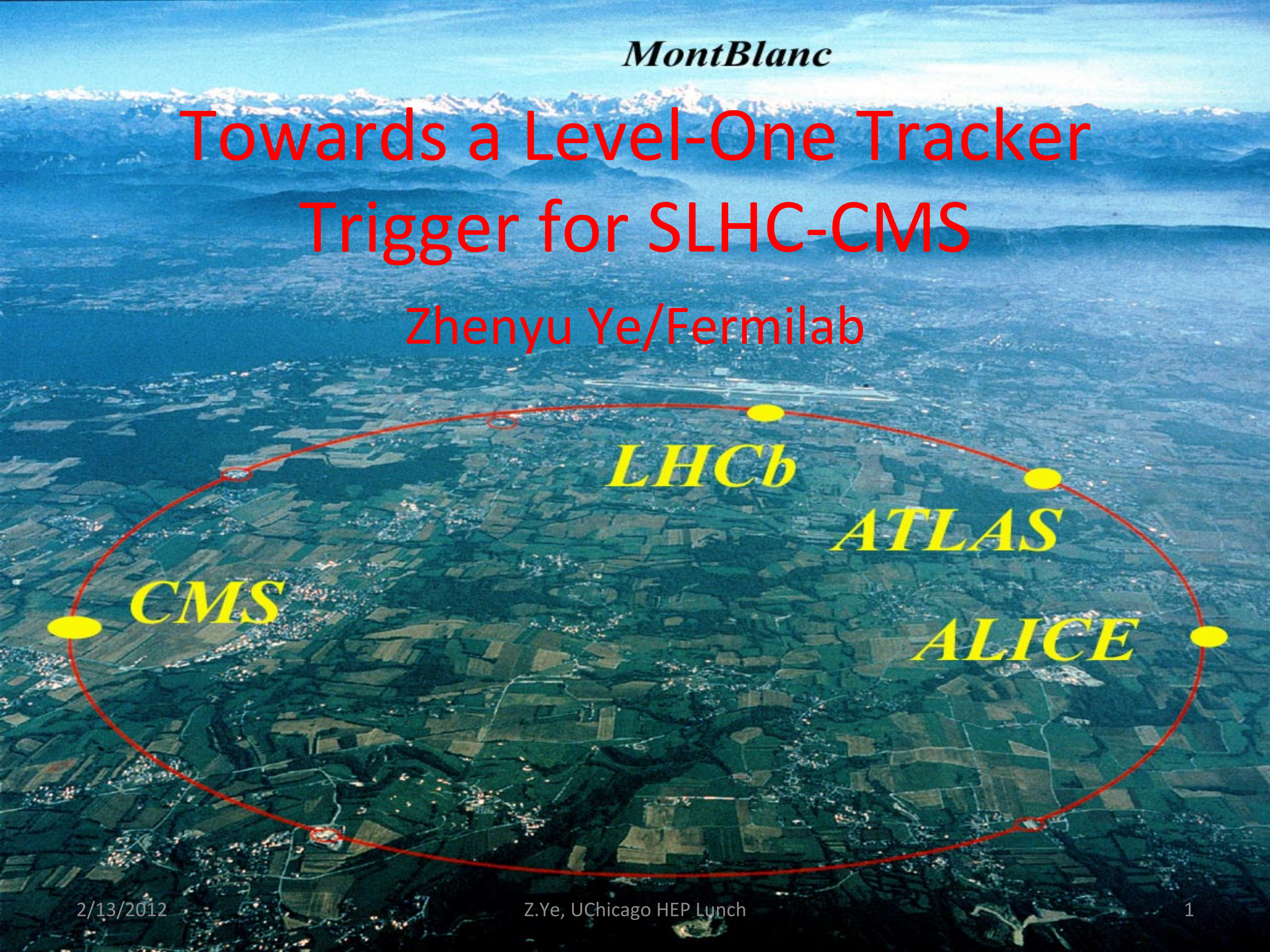
Towards a Level-One Tracker Trigger for SLHC-CMS

Zhenyu Ye/Fermilab

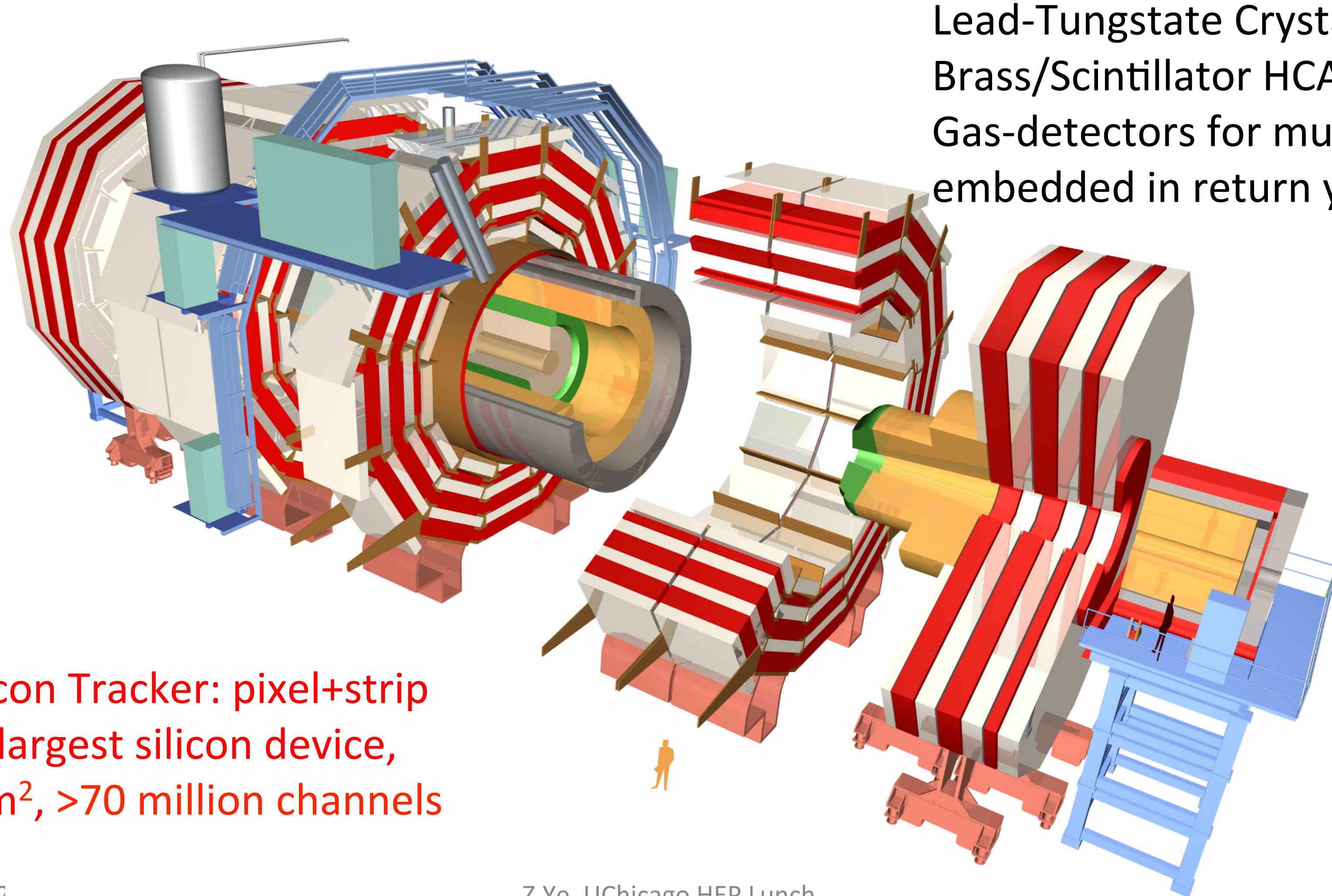


Outline

- Introduction
- Level-One Tracker Trigger for SLHC-CMS
  - VICTR: **V**ertically **I**ntegrated **C**MS **Tr**acker ASIC
  - Oxide Bonding and Active Edge Silicon Sensor
- Summary and Outlook

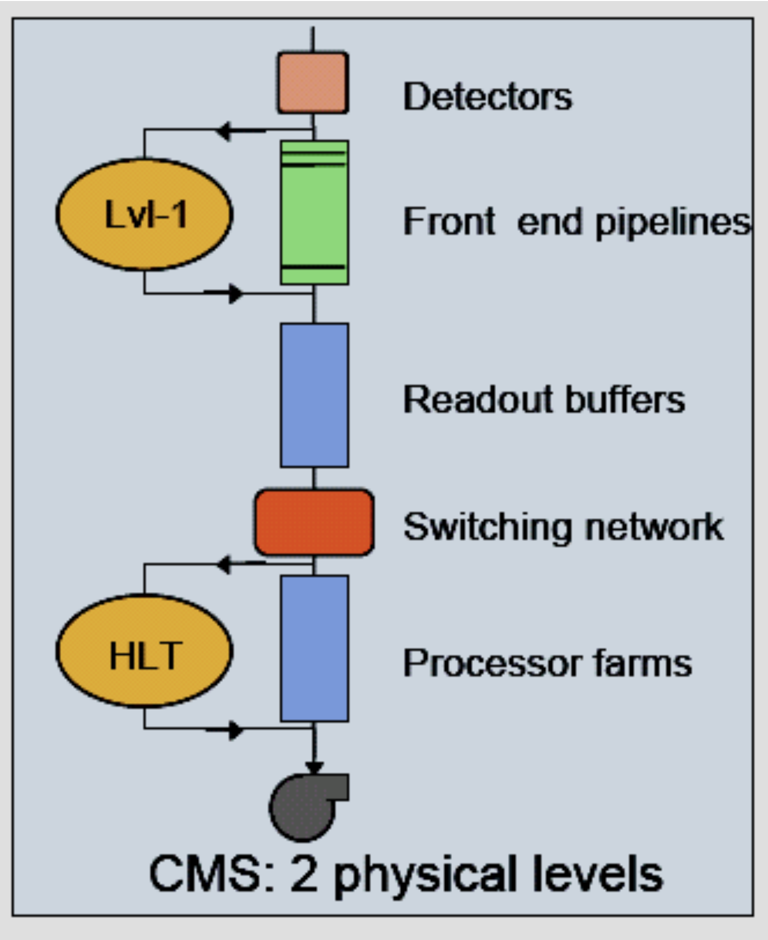
The CMS Detector

3.8 T solenoida B field;
Lead-Tungstate Crystal ECAL;
Brass/Scintillator HCAL.
Gas-detectors for muons embedded in return yoke.



All Silicon Tracker: pixel+strip
world largest silicon device,
~200 m^2, >70 million channels

The CMS Trigger System



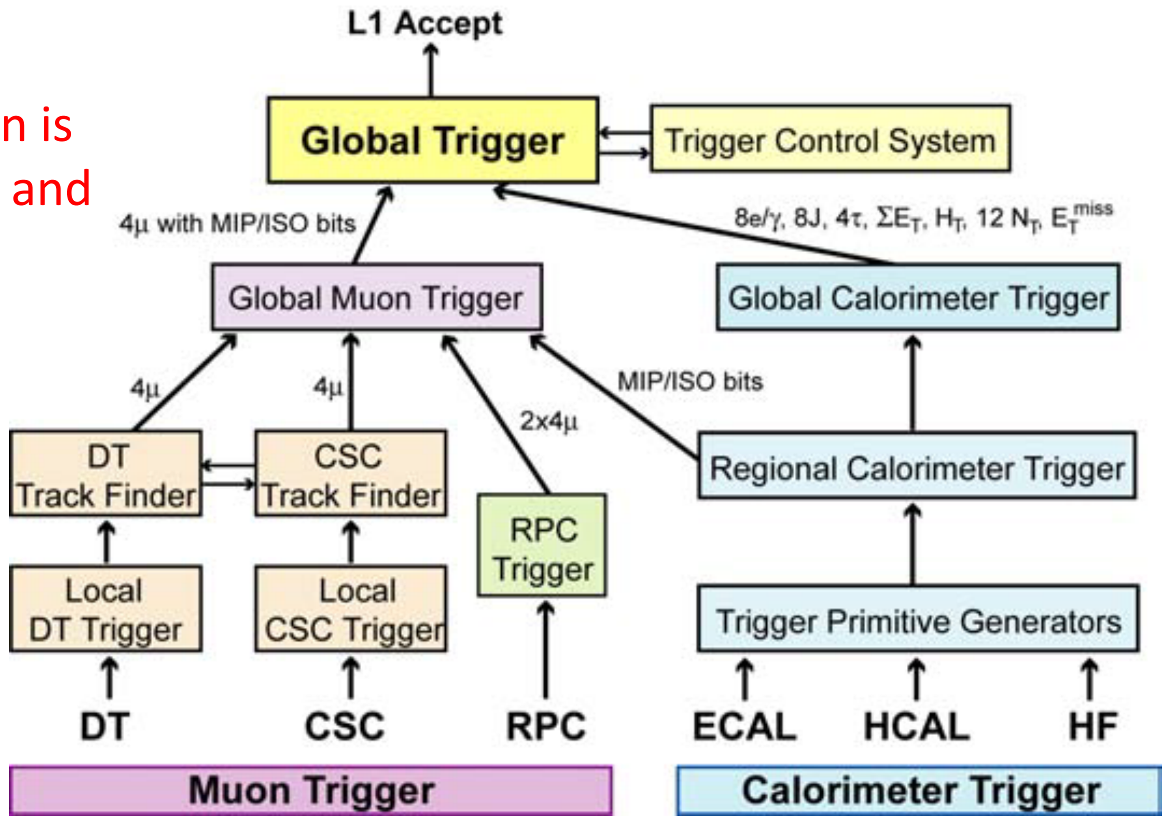
- Level-1 Trigger: Custom made hardware processor.
- High Level Trigger: PC Farm using reconstruction software and event filters similar to the offline analysis.

- 40 MHz input rate at L1
- 100 KHz input rate for HLT
- 100 Hz written at the output

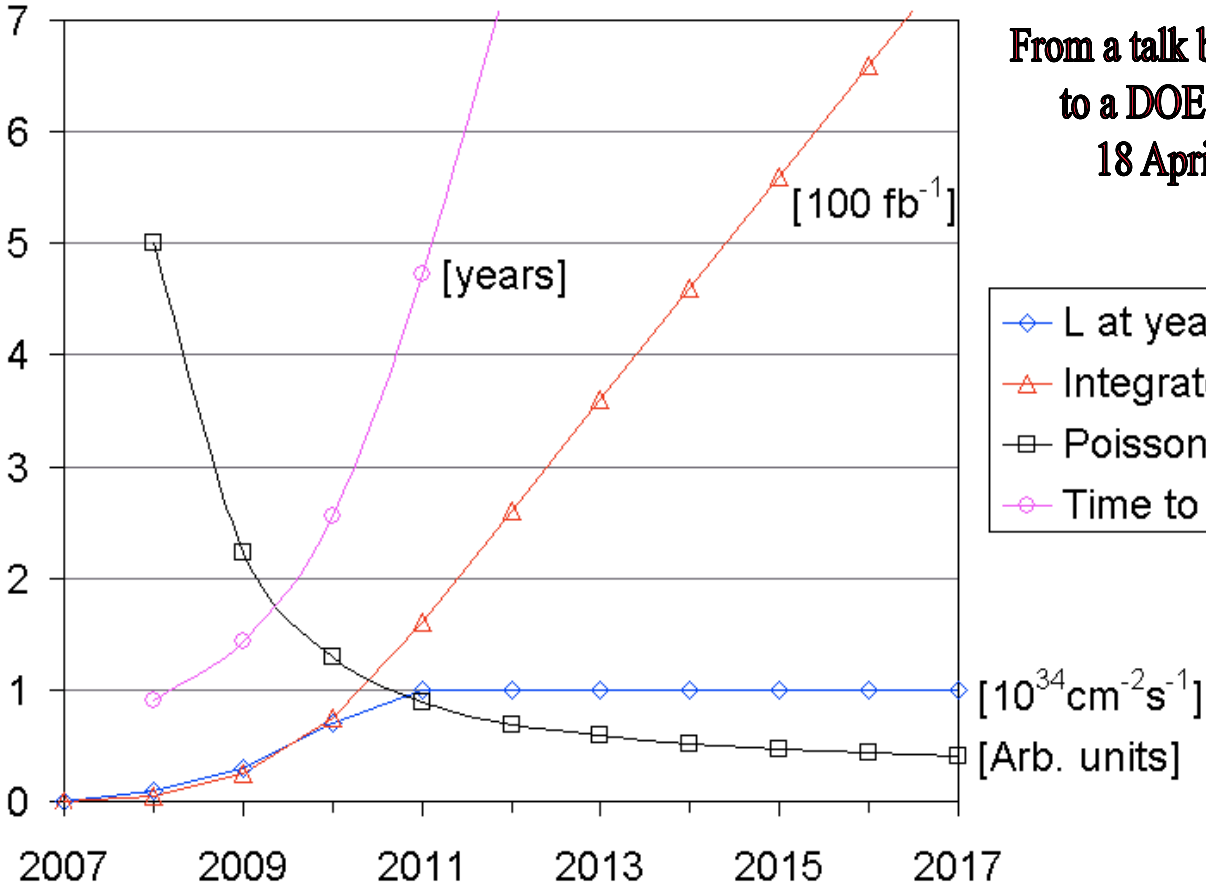
- 128 Bx = 3.2 μsec L1 latency
- Event Size 1-2 Mbytes
- Impossible to read out all tracking channels at L1

The CMS L1 Trigger System

- Current L1 trigger decision is based on the calorimeter and muon detector.
- At L1 we trigger on:
  - high E_t $e^{\pm}/\gamma$
  - high P_t muons
  - high E_t jets
  - high E_t tau's



The SLHC



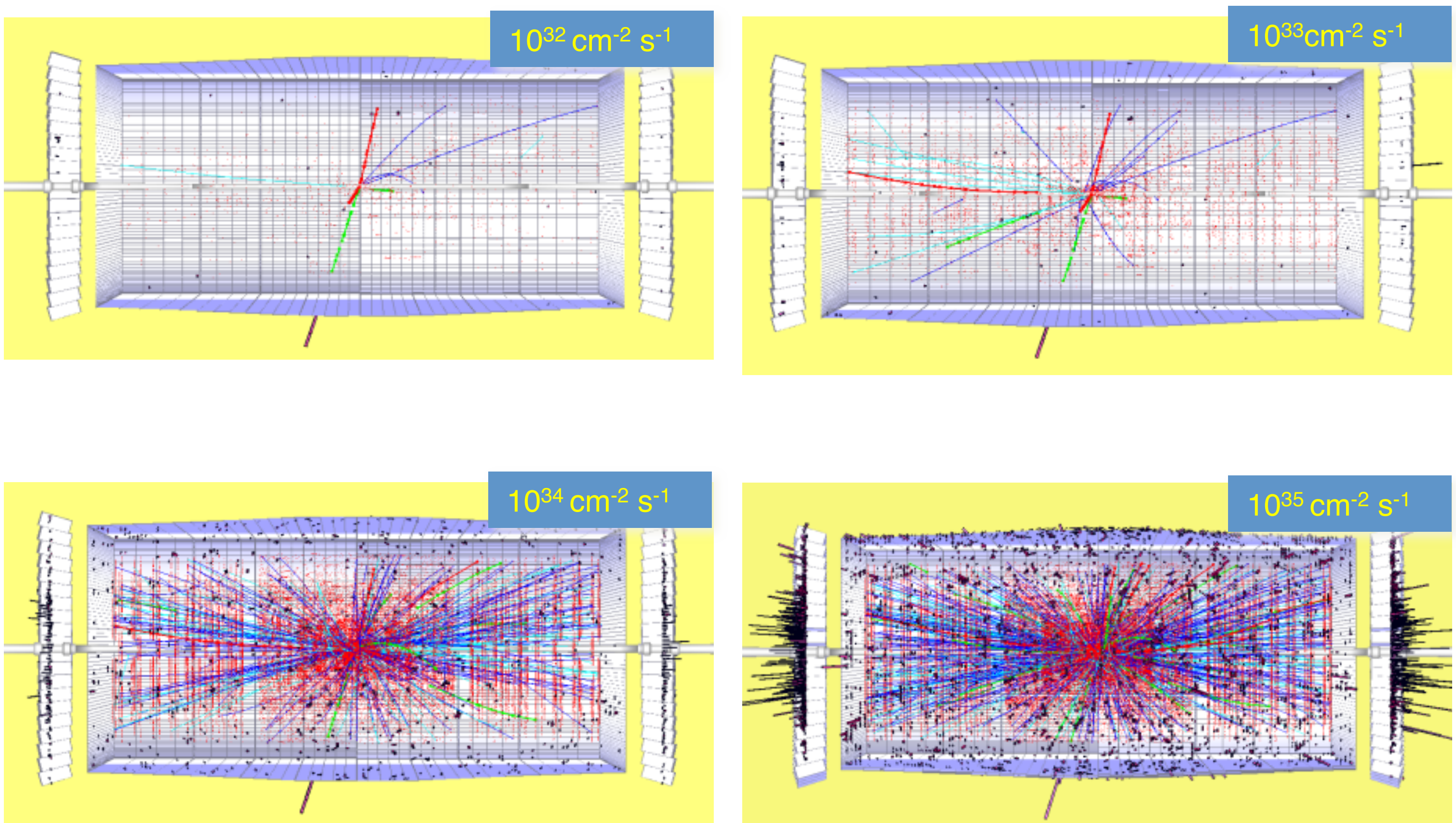
From a talk by Jim Strait
to a DOE Meeting
18 April 2003

By 2018 the gain of running LHC longer will be limited

A luminosity upgrade is planed thereafter….

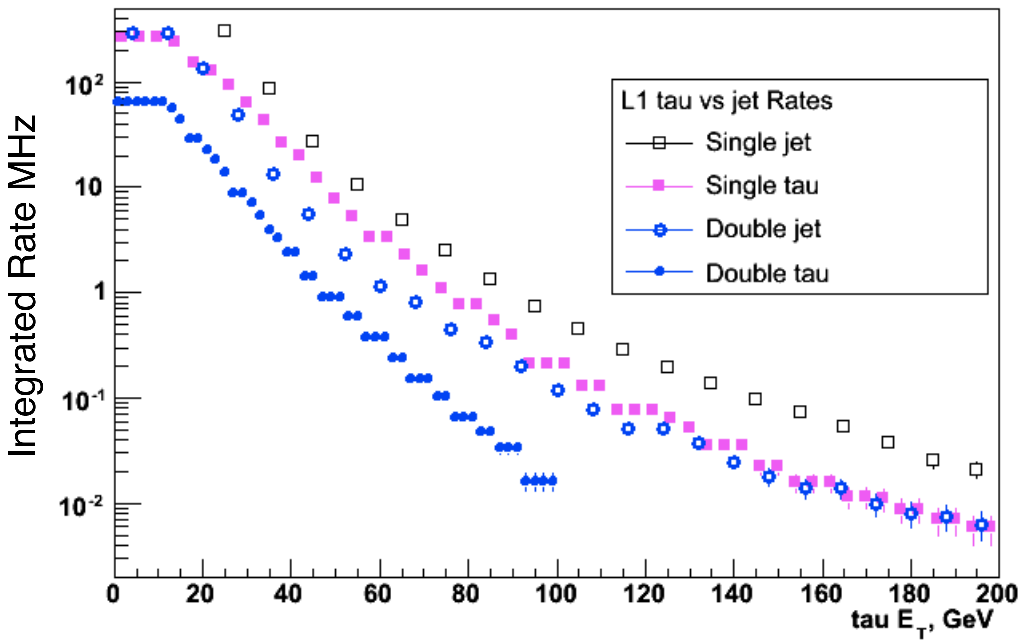
The SLHC

- 200-400 interactions/25 ns crossing at the SLHC

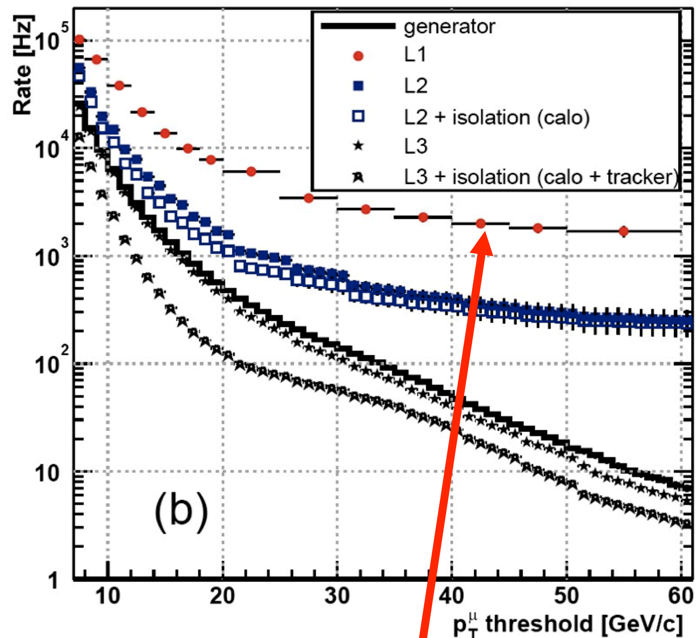


L1 Trigger Rate at SLHC

Jet and tau triggers at SLHC



Muon-trigger rates at LHC



- At the SLHC, electron, jet, tau and muon triggers will fire in the MHz region (with the LHC thresholds). Keeping the same thresholds as at LHC may be desirable if one wants to study possible LHC signals with more statistics.
- Even if one wished to raise threshold it would not help as shown in the muon trigger case.

L1 Tracker Trigger for SLHC-CMS

- CMS at the SLHC
  - L1 trigger rate based on calorimeter and muon detector will saturate
  - Tracking info has to be included for L1 trigger decision
- Need a track trigger to be able to
  - Identify and provide a Z vertex resolution of ~1mm for tracks with p_T above ~2.5 GeV at L1 (e/μ/tau track isolation, particle flow jet)
  - Identify and provide a Z vertex resolution of ~1mm for tracks with p_T above ~15 GeV at L1 (e/μ track match)
  - provide full event readout upon HLT trigger accept
- Track p_T and Z need to be determined "locally"
  - Unacceptable power and bandwidth required to transmit all hit information from the tracker to an external trigger processor

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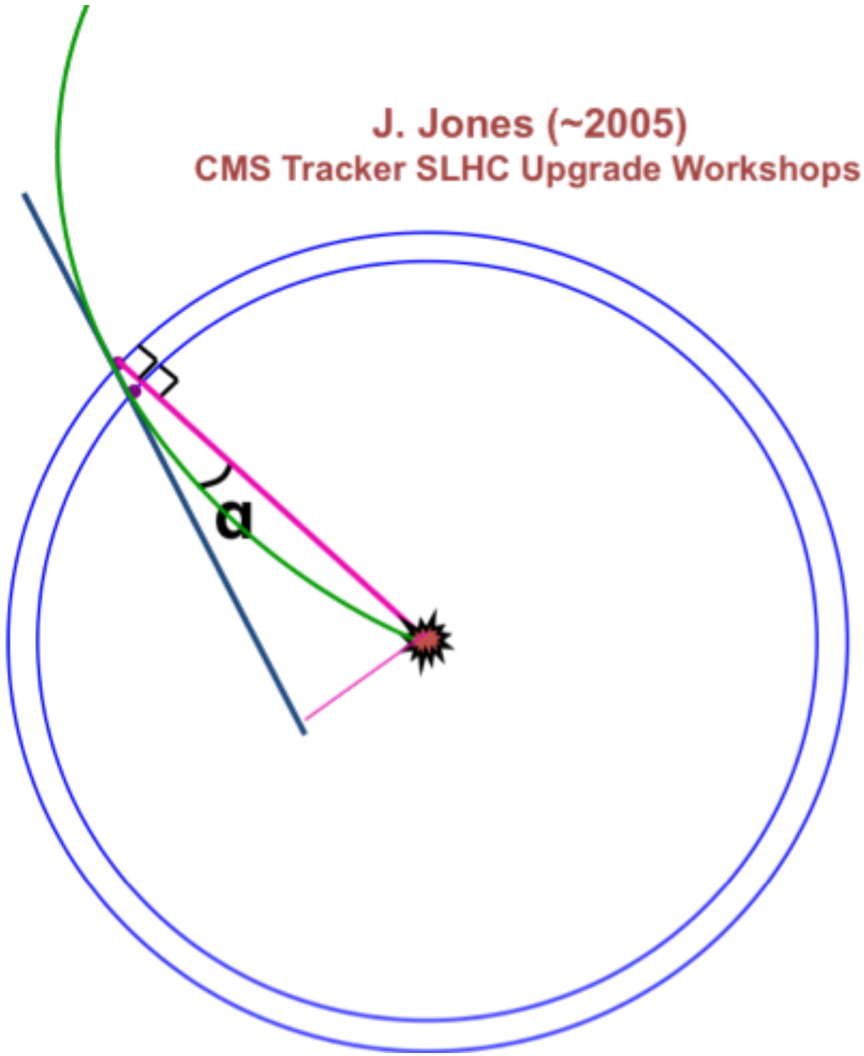
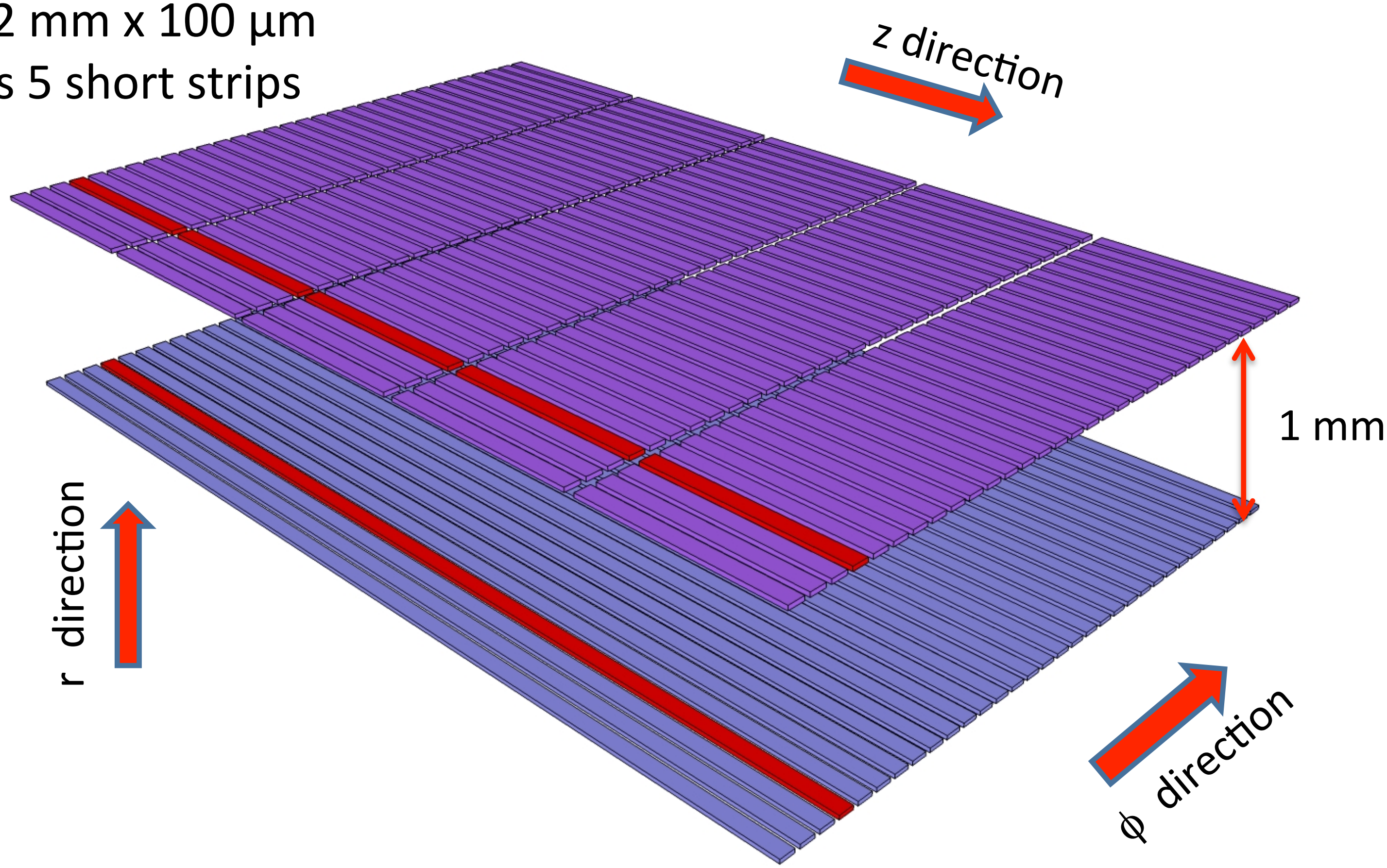


A filter for high p_T track hits based on the impact parameter of the hits on two adjacent layers of silicon detectors.

Silicon Sensors for Tracker Trigger

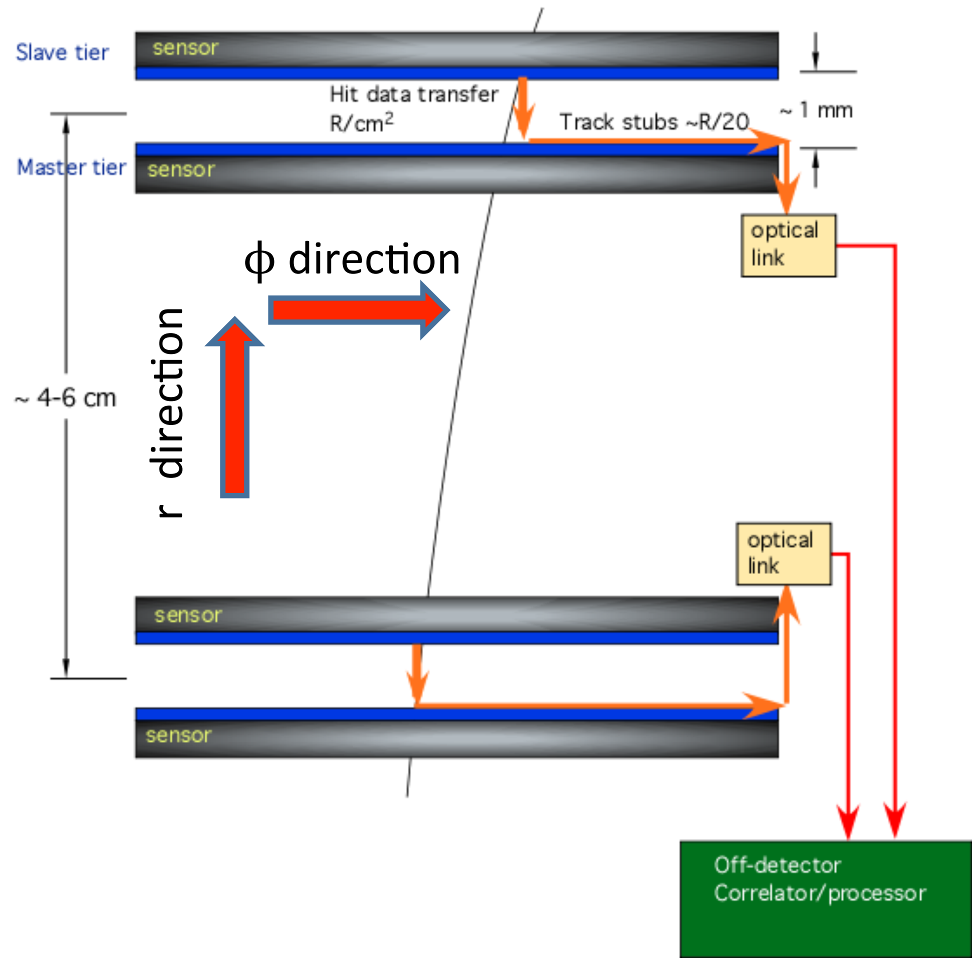
Don't need fine Z resolution on both layers:

- long strip: 5-10 mm x 100 µm
- short stip: 1-2 mm x 100 µm
- 1 long strip vs 5 short strips



L1 Track Trigger Design

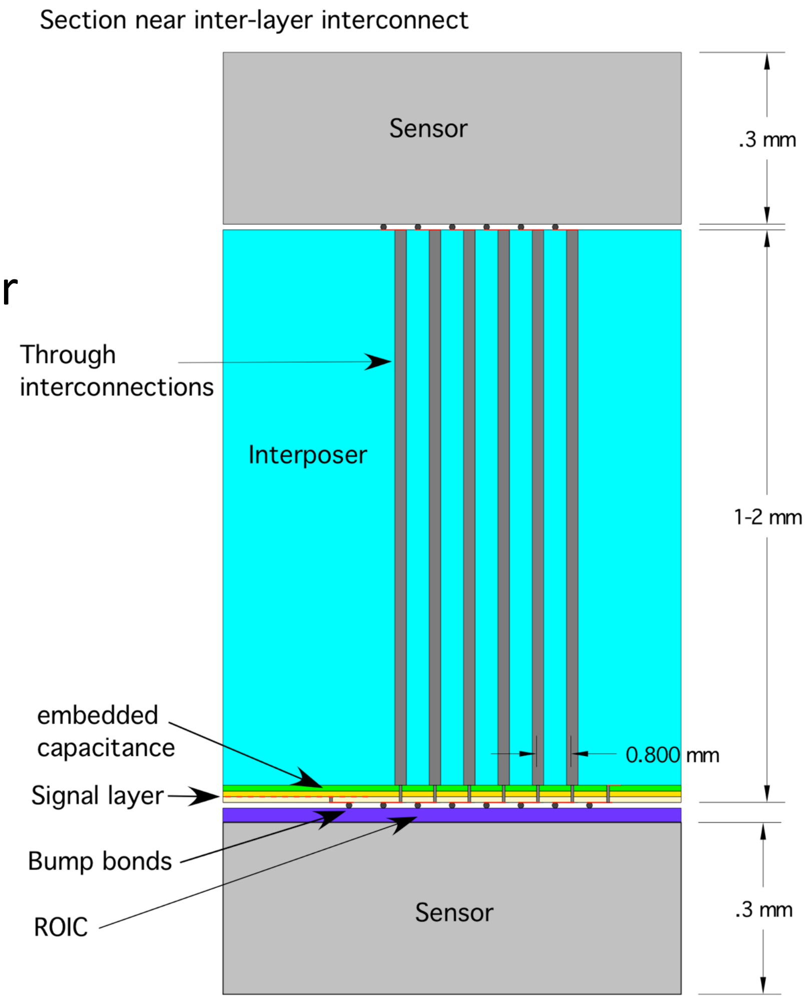
- Pixelated silicon sensor to allow both ϕ and Z position measurement for hits on the detector.
- Two layers of silicon sensors separated by ~1mm for local high p_T track hits filtering and track stub formation
- Multiple double-layers for track reconstruction



L1 Track Trigger Design

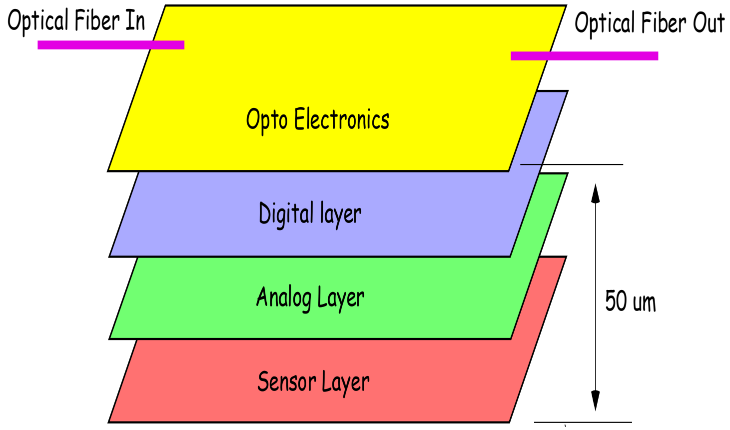
One single readout chip connects to both the top and bottom sensors

- Analog information from the top sensor is passed to the ROIC through a PCB interposer
- reconstruct hits locally for each sensor
- correlate hits from the top and bottom sensors to form track stubs
- provide the reconstructed track stubs for L1 track reconstruction
- provide the full event info upon L2 accept

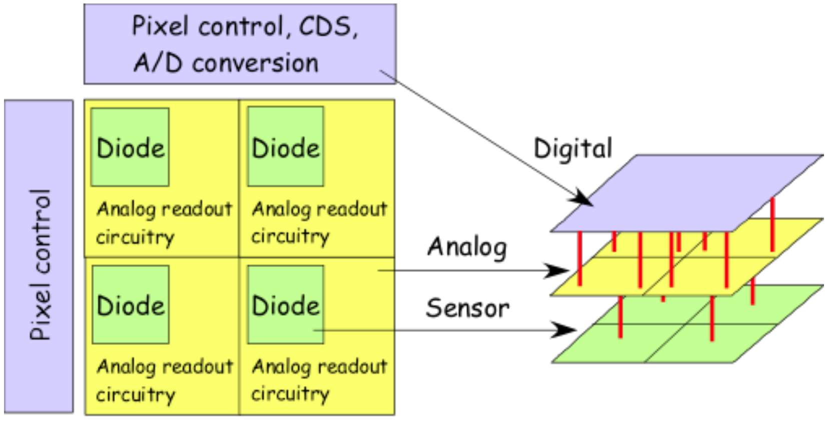


How to Build – 3D Integration

- A **vertically (3D) integrated circuit** comprised of 2 or more layers of CMOS devices which have been thinned, bonded, and vertically interconnected to form a "monolithic" circuit. These layers can be devices made in different technologies.
- A major direction in semiconductor industry:
  - Reduces trace length; Reduces R, L, C;
  - Improves speed; Reduces interconnect power, crosstalk;
  - Reduces chip size; Processing for each layer can be optimized.



Designer's Dream

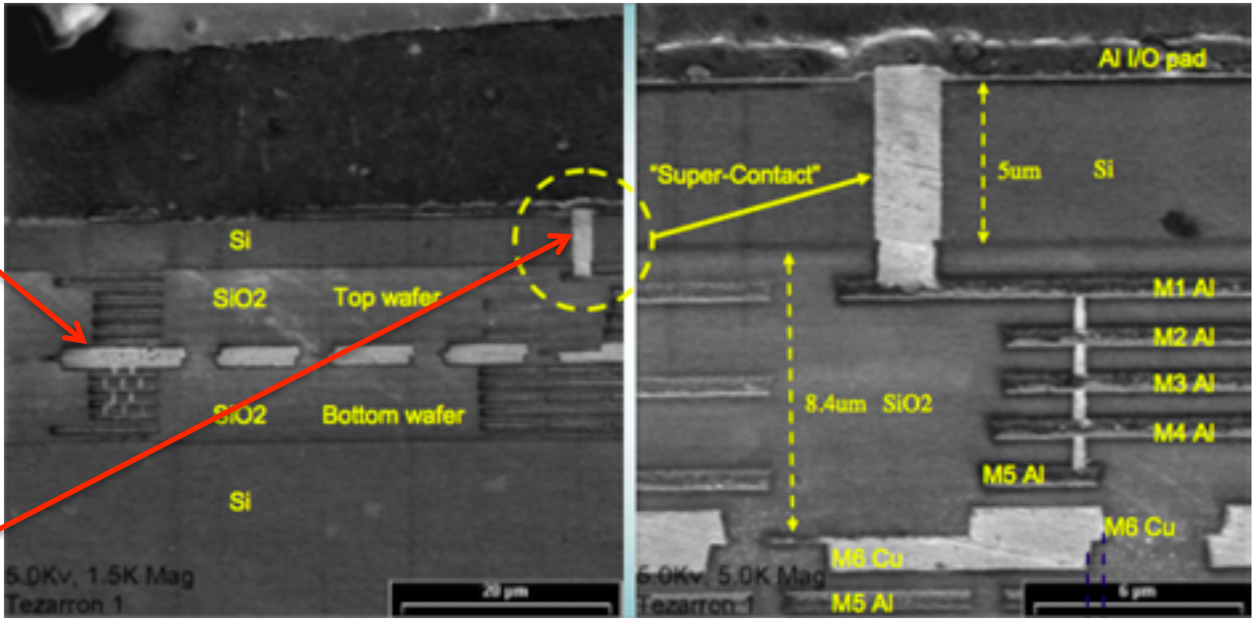


Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

How to Build – 3D Integration

- Bonding between layers
  - Cu-Cu
  - Si Oxide
  - Cu-Tin
  - Polymer/adhesive
- Wafer thinning
  - grinding, lapping, etching, CMP
- Through silicon via formation
- High precision alignment



Cu-Cu bonded two-tier IC (Tezzaron)

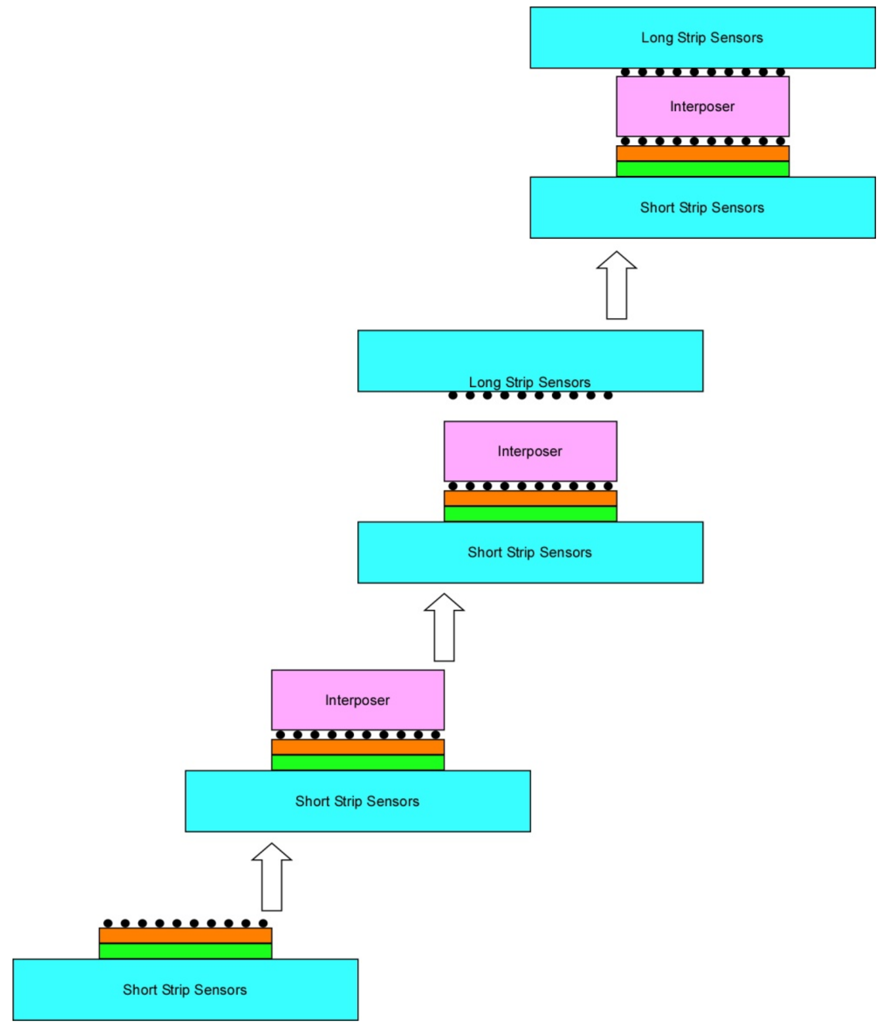
How to Build – 3D Integration

4 The top sensor is bump-bonded to the PCB Interposer making a complete device.

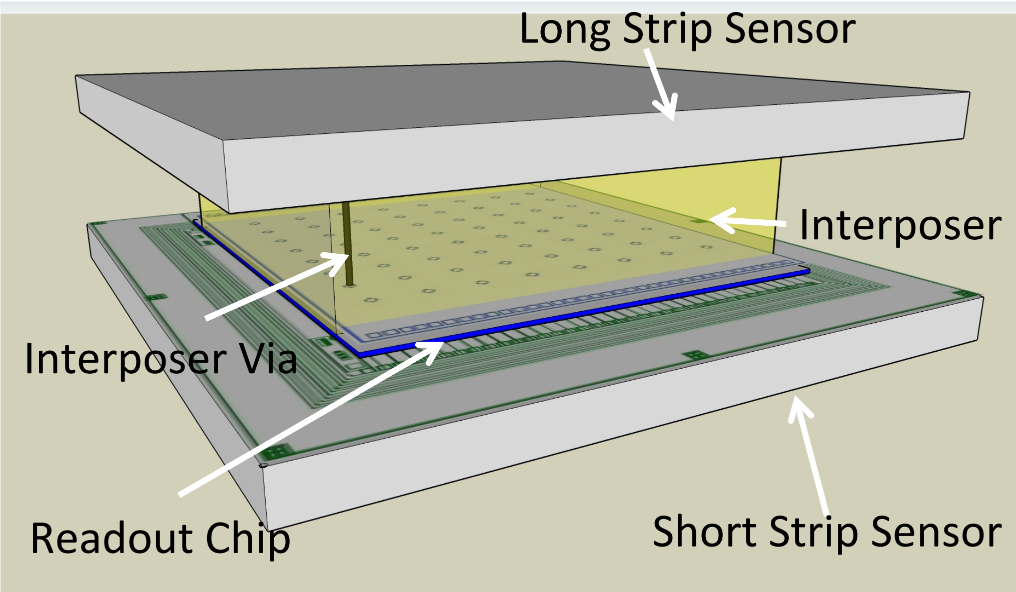
3 Bumps are placed on the top sensors

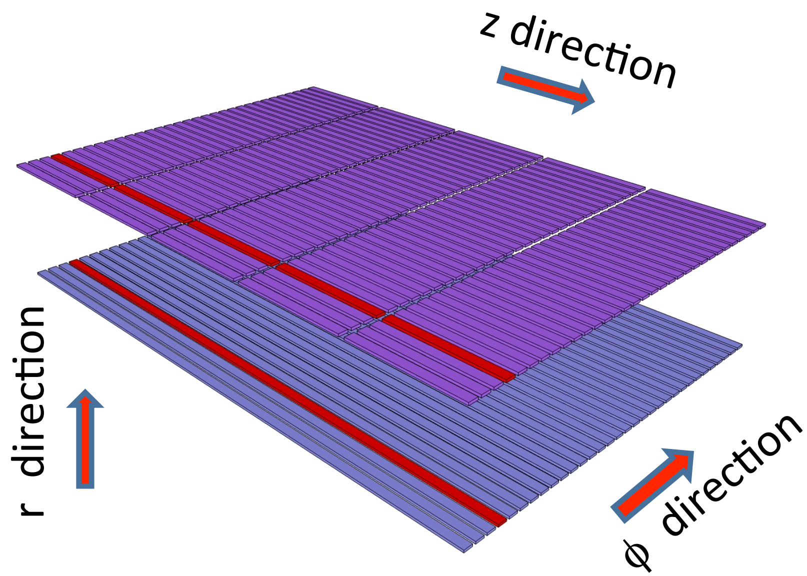
2 The PCB Interposer is bump-bonded to the 3D ROIC

1 The 3D ROIC is oxide-bonded to the bottom sensor and then thinned.



L1 Track Trigger Design





One single readout chip for two silicon sensors, one sensor connected from the top through the interposer and the other from the bottom

- The top sensor has "long" strips (5mm*0.1mm)
- The bottom sensor has "short" strips (1mm*0.1mm)

L1 Track Trigger Design

- Module design assumes a 5x6 array of chips.
- There is a placement yield for each chip, unless this yield is very close to 100% this design will be too costly
- Use known good sensor/ROIC and high yield bump bonds to connect to PCB
- Smaller modules are problematic because saw cut edges on normal silicon are sources of leakage current. Usually stay 3x depth away to limit leakage current - creates dead areas
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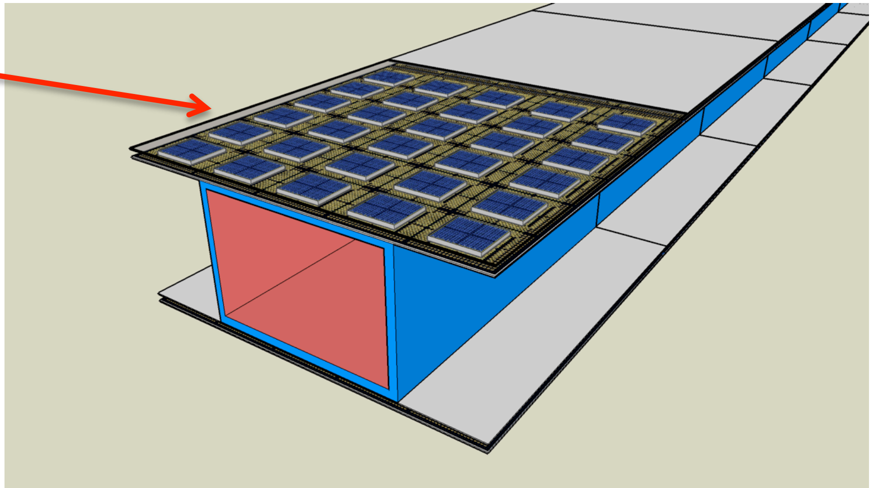

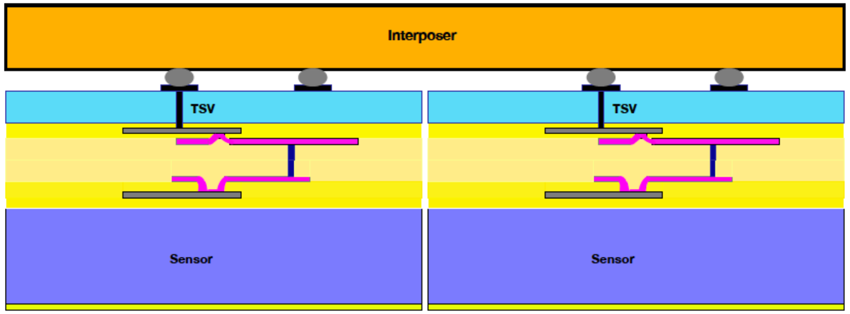

Technical Feasibility

Challenges	Approach
A CMOS technology which can communicate with top and bottom sensors (through silicon vias)	Demonstrate technology with 0.13 micron Tezzaron 3D process (VICTR chip) and oxide bonding with Ziptronix (BNL wafer)
An interposer technology with low mass	Develop low mass PCB-based interposers
A chip and module design which can process a full event every 25 ns	a test chip to demonstrate data flow
Modules which can be fabricated with acceptable cost and yield.	R&D on using active edge sensors combined with 3D chips
Physics performance	Detector studies and simulation

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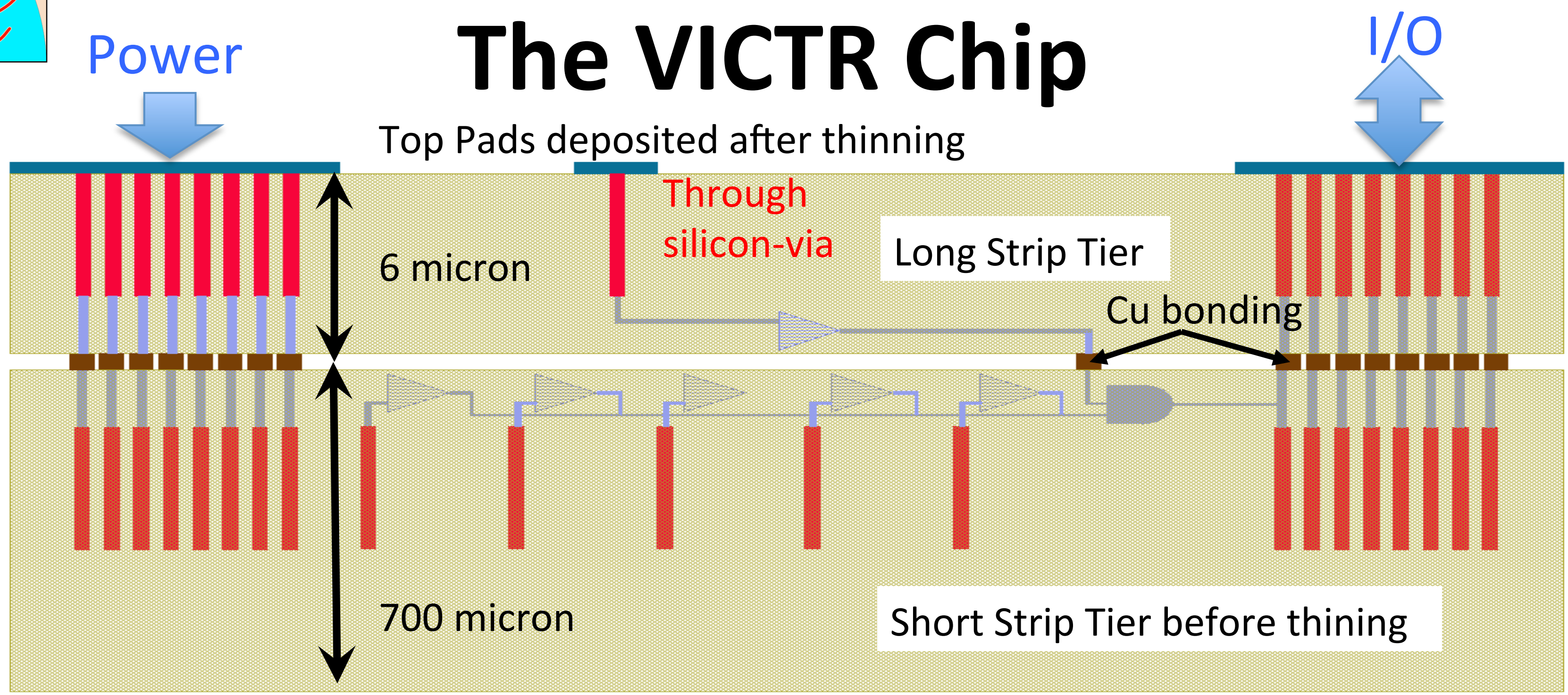
The VICTR Chip

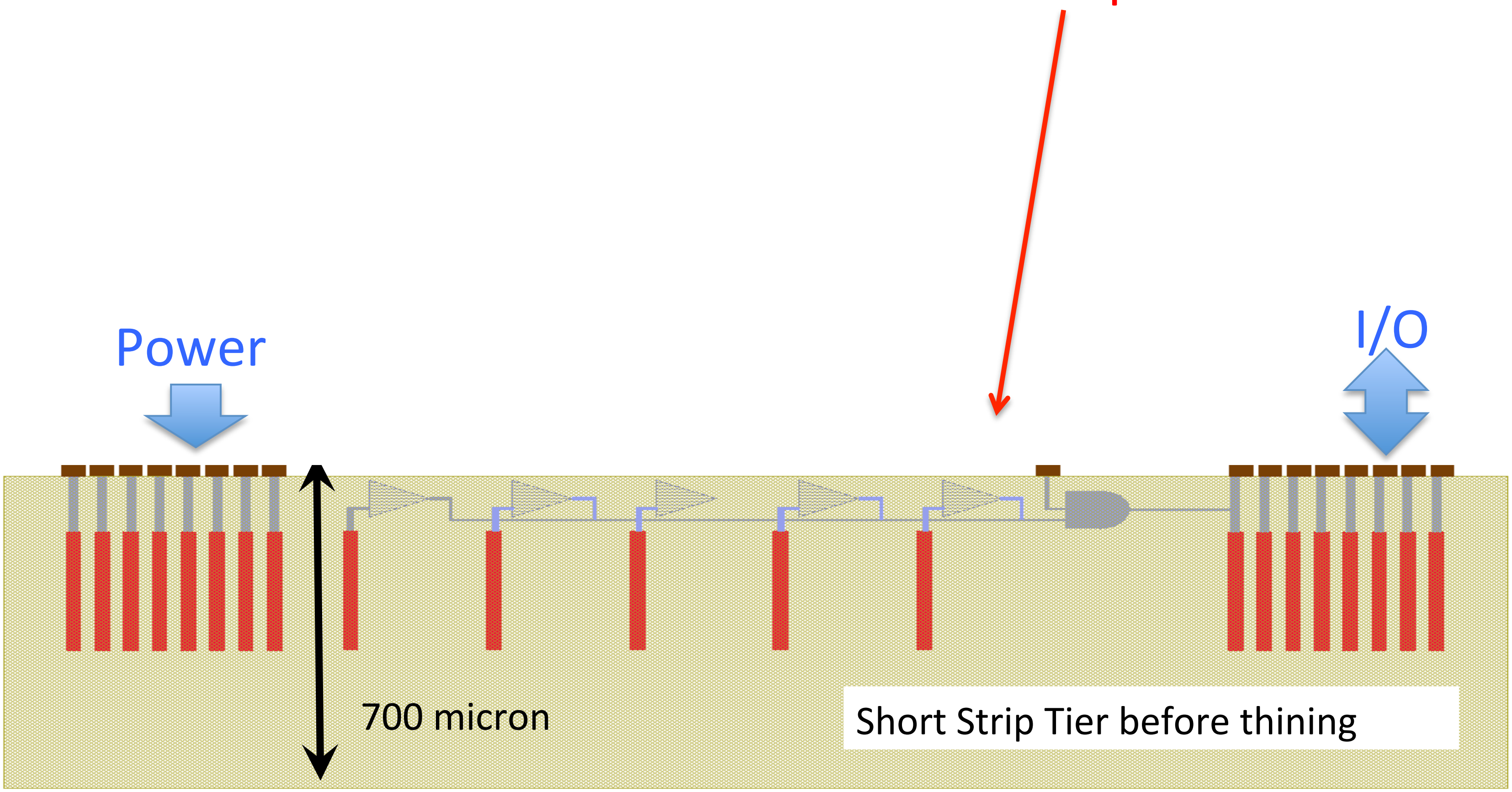


VICTR chip: two tiers vertically integrated with Cu-Cu bonding

- Each tier has its own set of shifter registers, digital-to-analog converters for frontend bias, and signal amplification-shaping-discriminating.
- Transfer discriminator outputs from the top long strip tier to the bottom short strip tier through TSVs and Cu-Cu bonding interconnects.
- Readout architechture exists in the bottom short strip tier only.

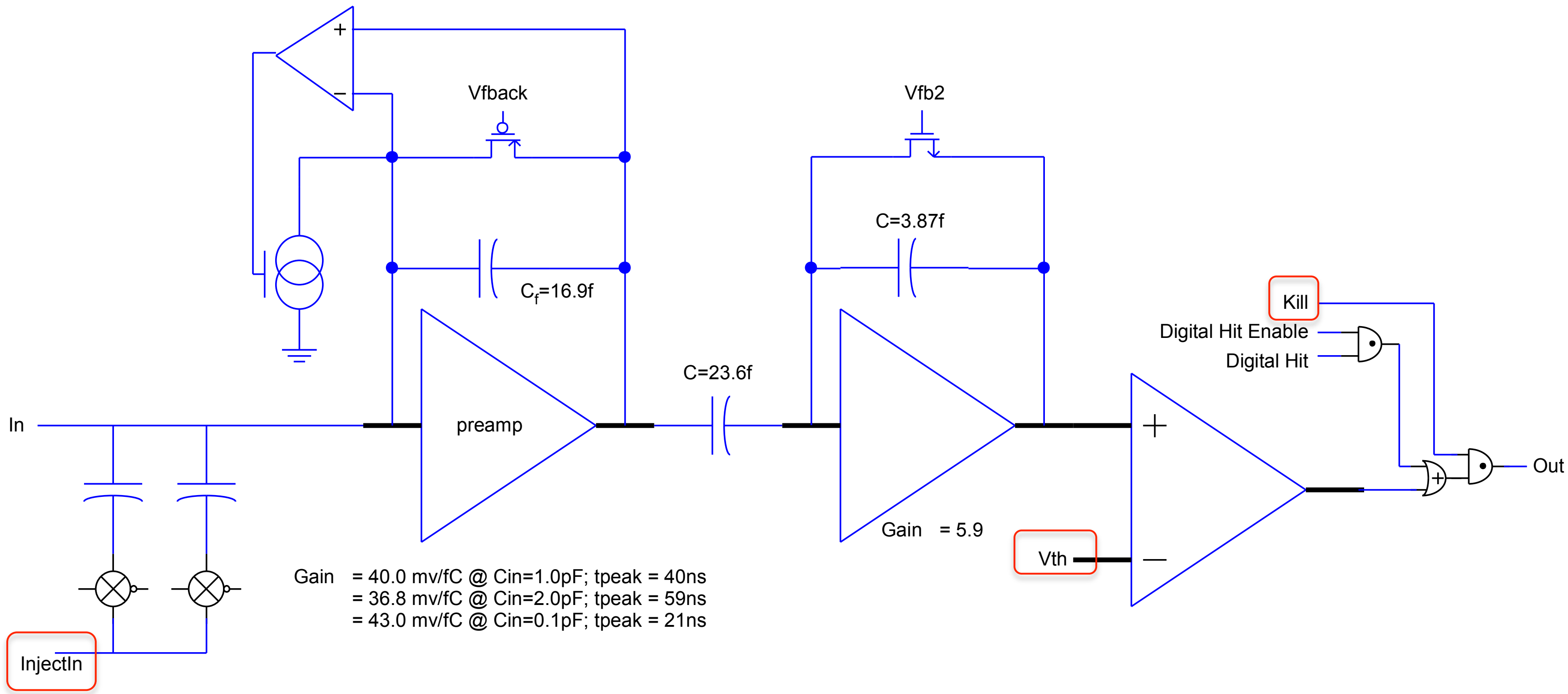
The VICTR Chip

- Two tiers vertically integrated with Cu-Cu bonding – “3D chip”.
- Each tier is able to work on its own – “2D chip”.



VICTR Chip Design

- Frontend A-S-D design from LBNL (A.Mekkaoui and J.Fleury)
- Control DACs design from CPPM (J.Clemens, P.Pangaud, S.Godiot)
- Readout architechture by Fermilab ASIC design group (J.Hoff et al.)

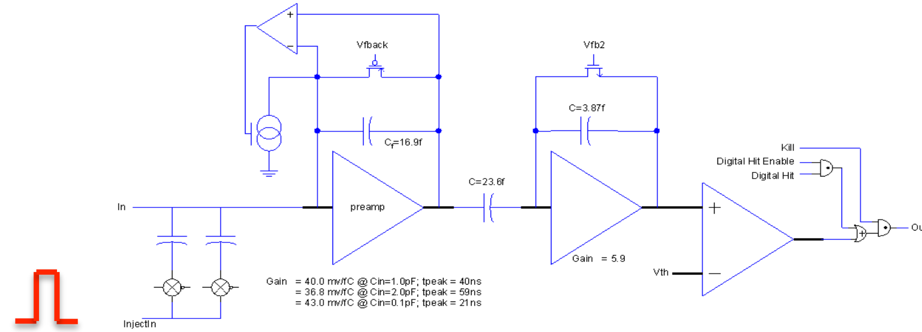


VICTR Chip Fabrication

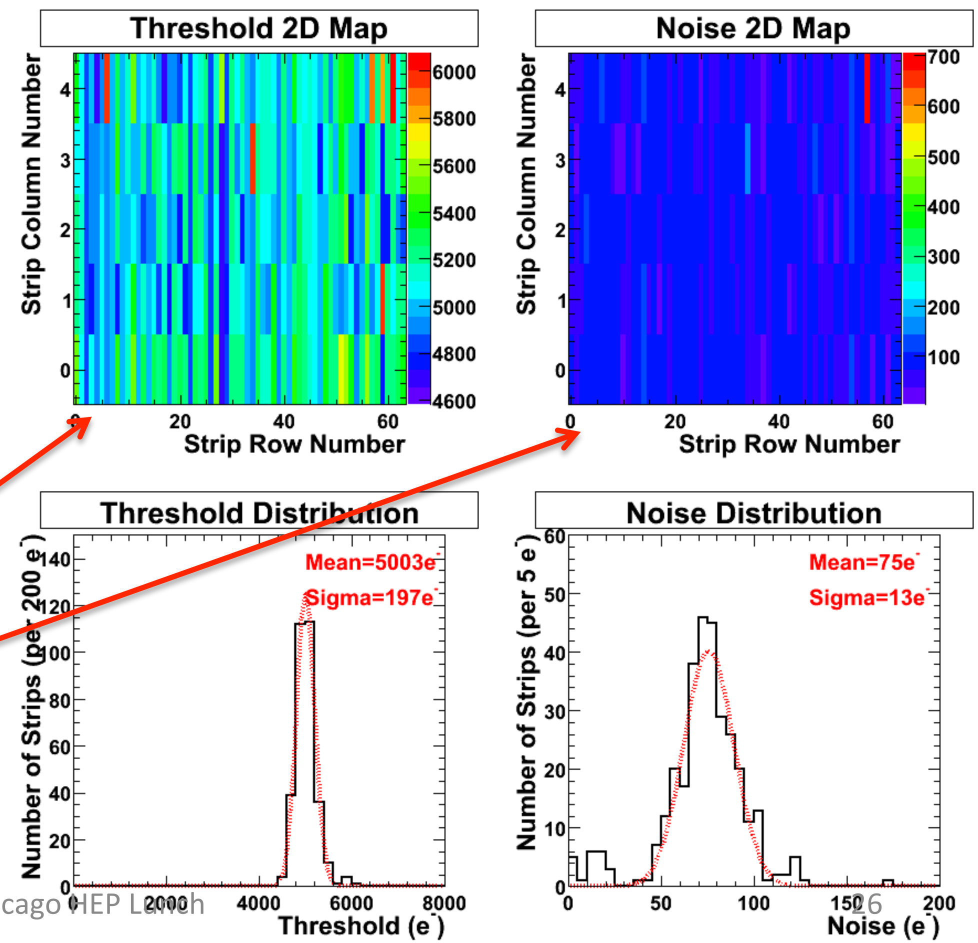
- Fabricated in the first HEP 3D multiproject run in Tezzaron 0.13 micron CMOS process.
- 2D chips tested in the summer.
- 3D chips received in September 2011.

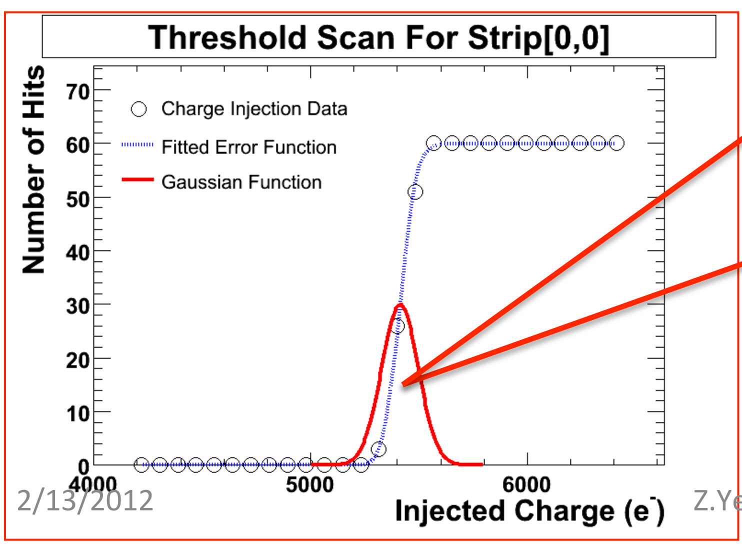
Tests for 2D Chips

- chip register download
- frontend bias control
- frontend ASD response
- backend readout

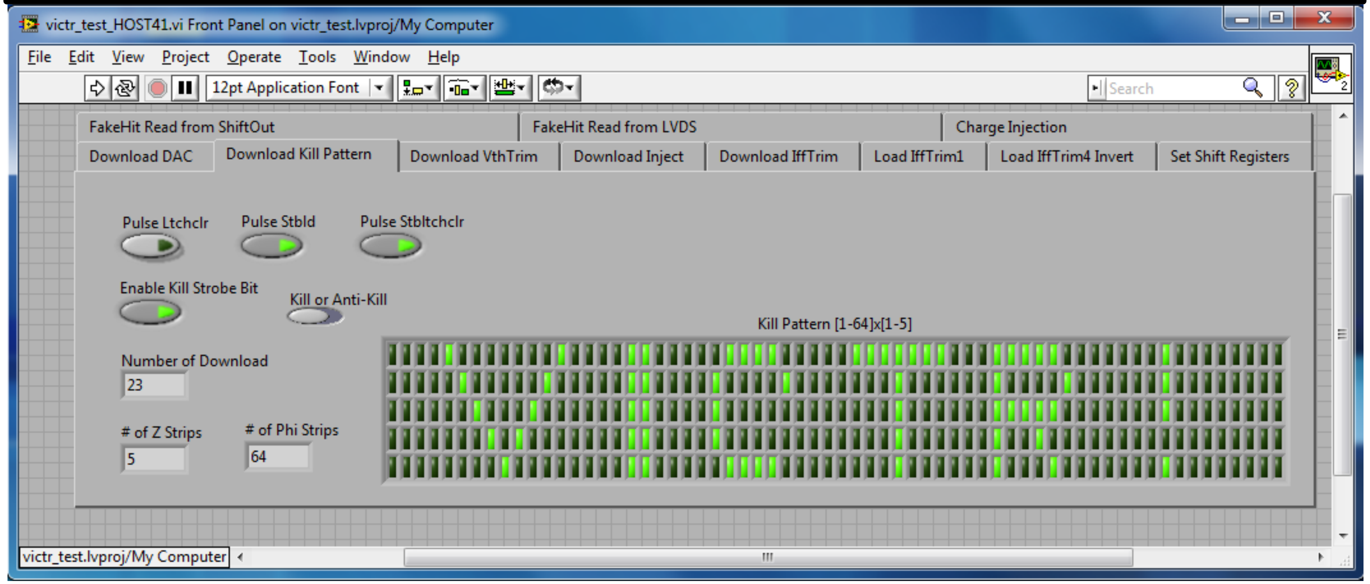


test pulse

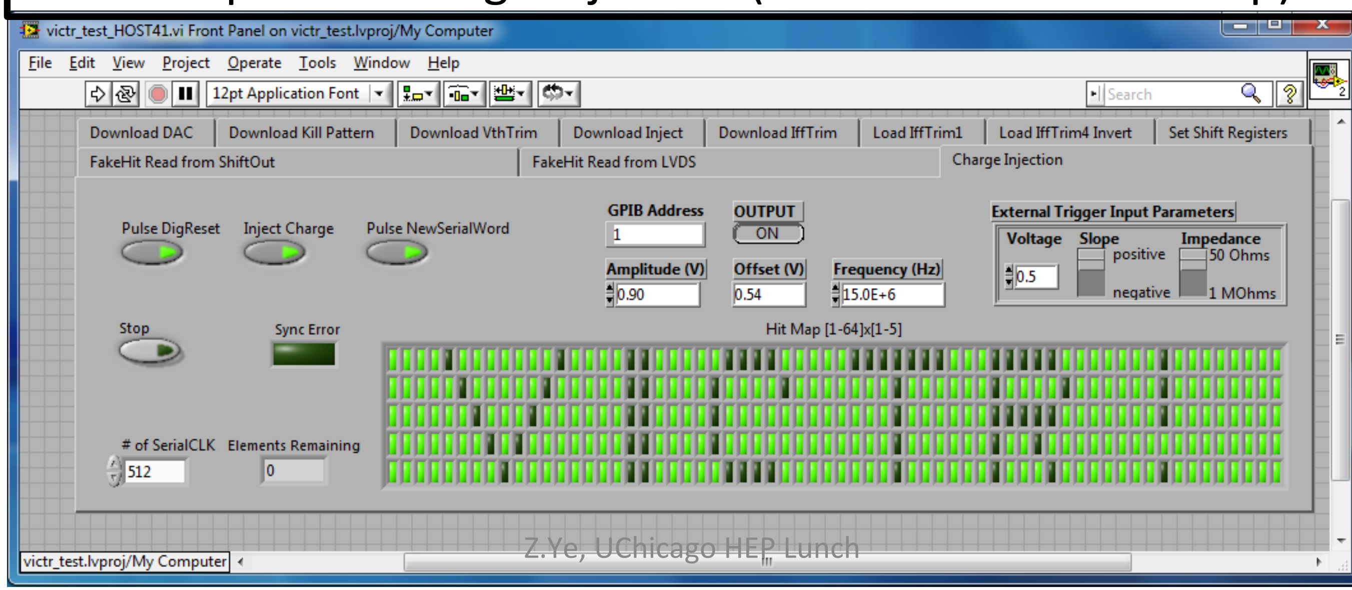




Kill Map Downloaded to Chip (to disable some strips)

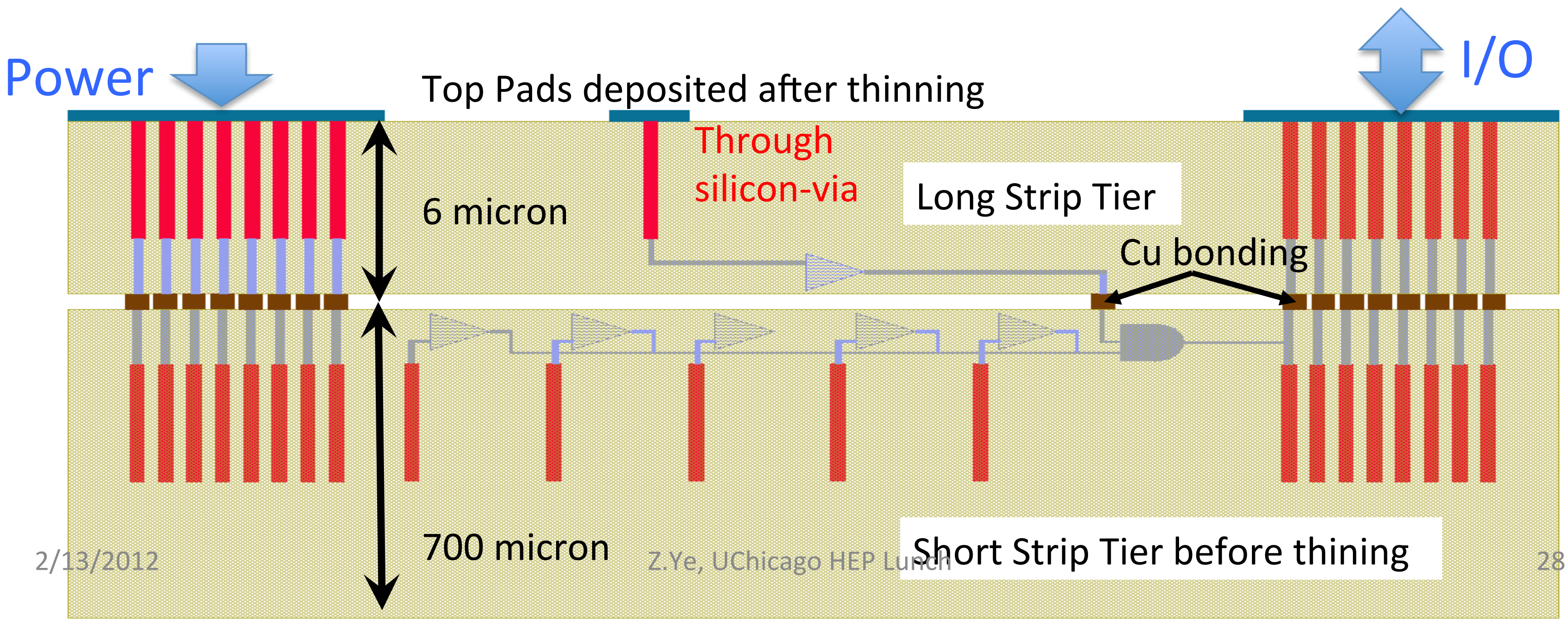


Hit Map from Charge Injection (consistent with kill map)

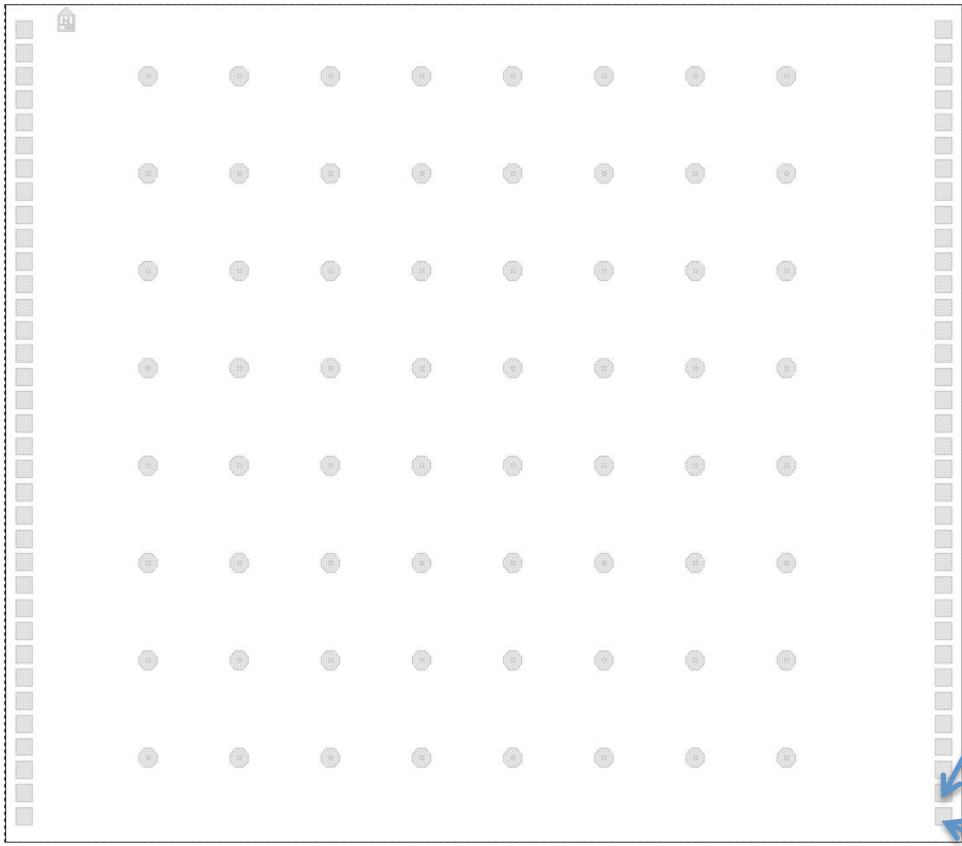


3D Chip Testing Results

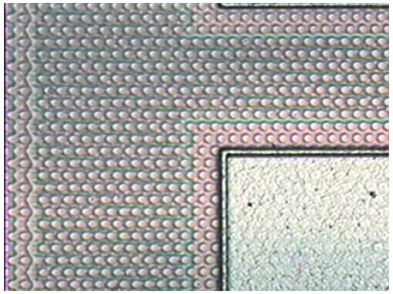
- Tested 3D chips in which either the short or the long strip tier was thinned.
- Shift register download ok for both long and short strip tiers for all 3D chips.
- Frontend bias control ok for both long and short strip tiers for all 3D chips.
- See discriminator outputs from the short strip tier in response to charge injection, but not from the long strip tier in response to charge injection.
- Similar A-S-D responses for the short strip tier among 3D chips, and to 2D chips.



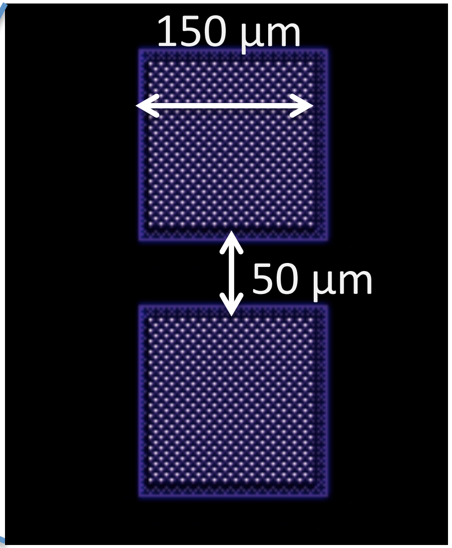
Interconnection Between Tiers



Connection between two tiers

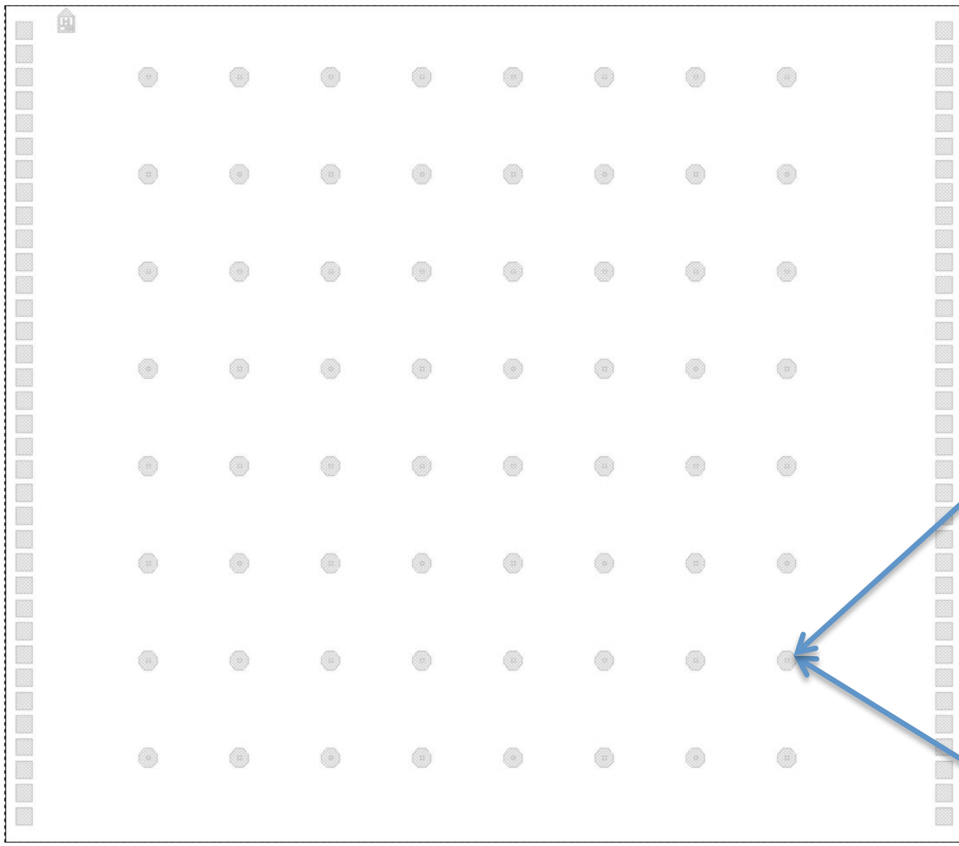


Cu-Cu bonding array

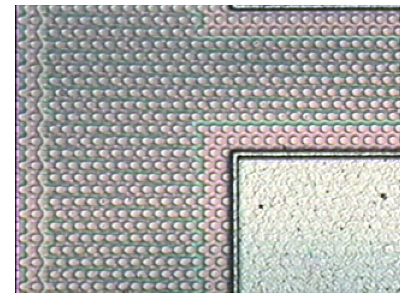


Connection for power or I/O pads

Interconnection Between Tiers



Connection between two tiers



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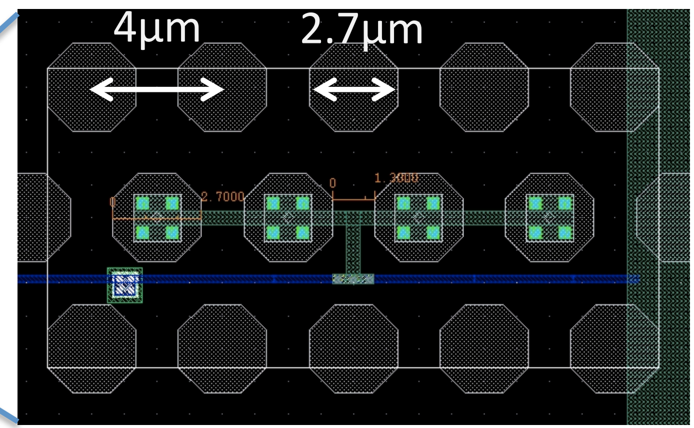
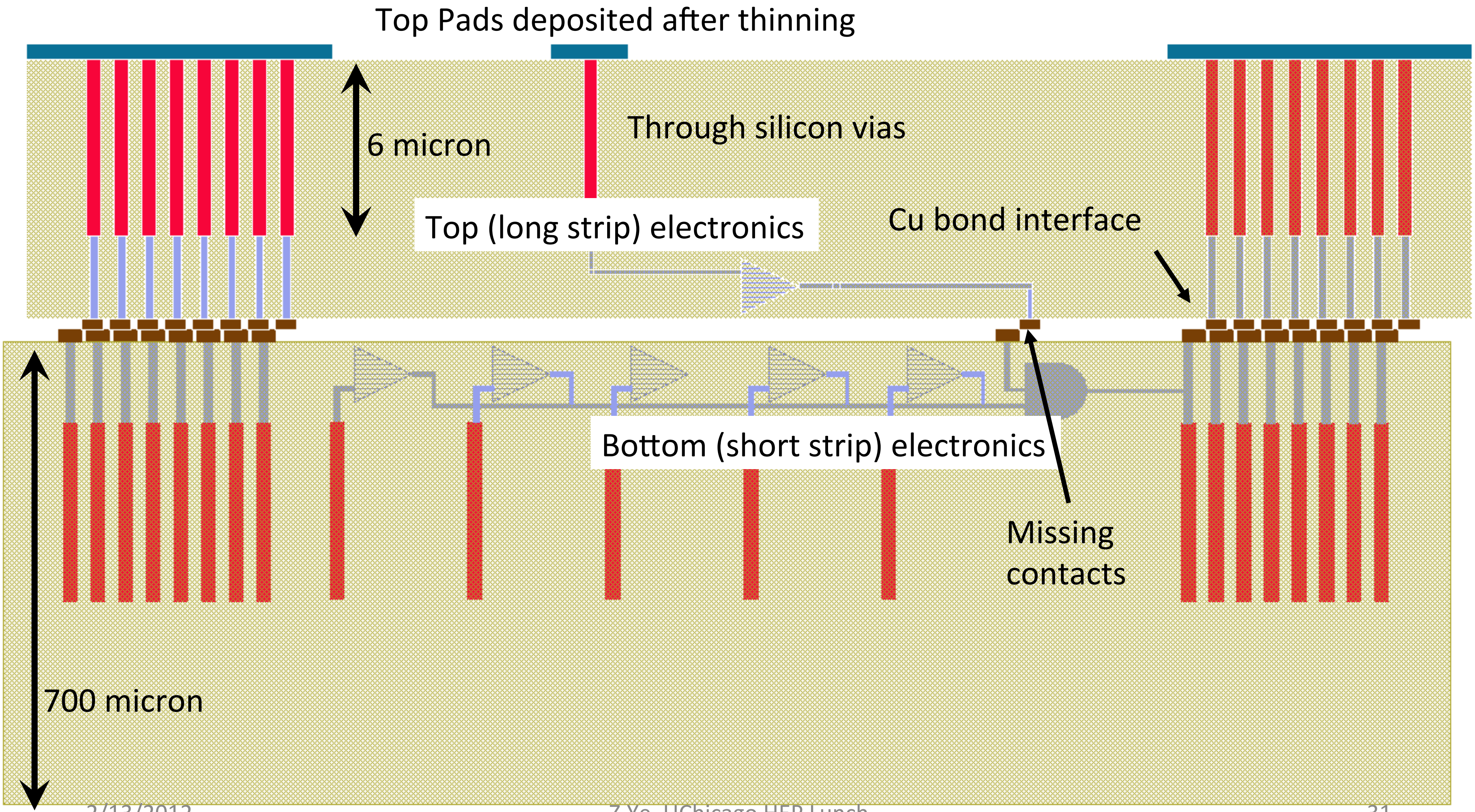
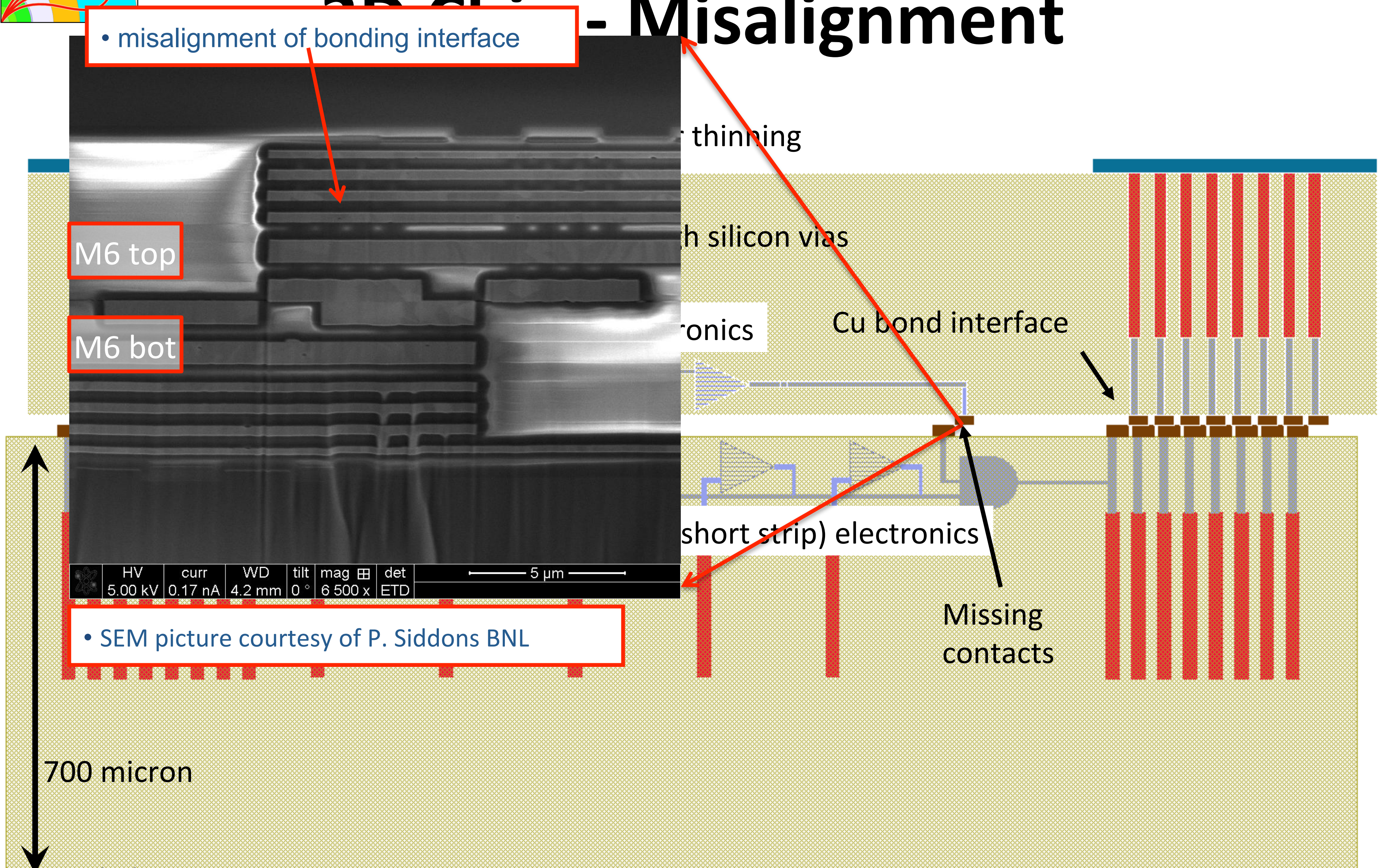


connection for discriminator output

3D Chip - Misalignment



- Misalignment



3D Chip Testing

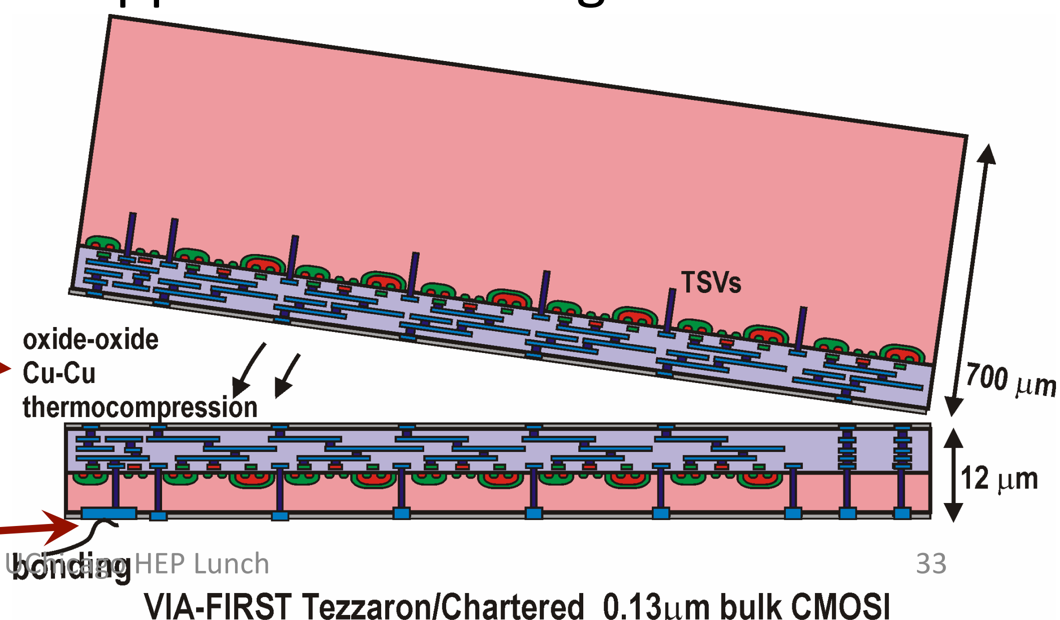
- First VICTR 3D Chip passed the smoke test
  - Download shift register between top and bottom layers works
  - Power controls work
  - Strip kill test working on short strip tier

This tests the backside thinning, exposure of the through-silicon-via, and Cu-Cu bonding, which *is all needed for the Track Trigger.*

- The first pair of bonded wafer appears to have alignment problems
- 12 more wafers (6 pairs) available for processing

Issues with this bond

This process is OK



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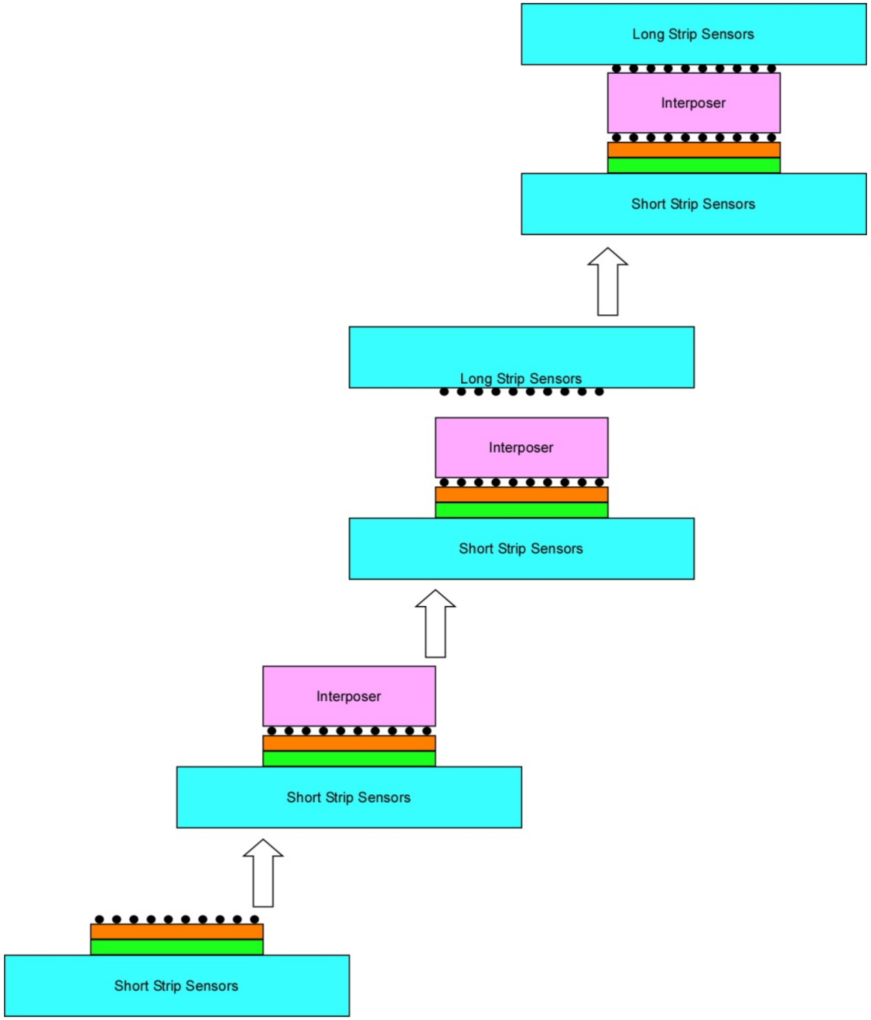


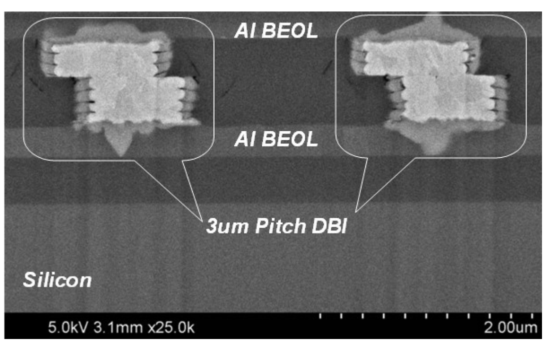
Oxide Bonding

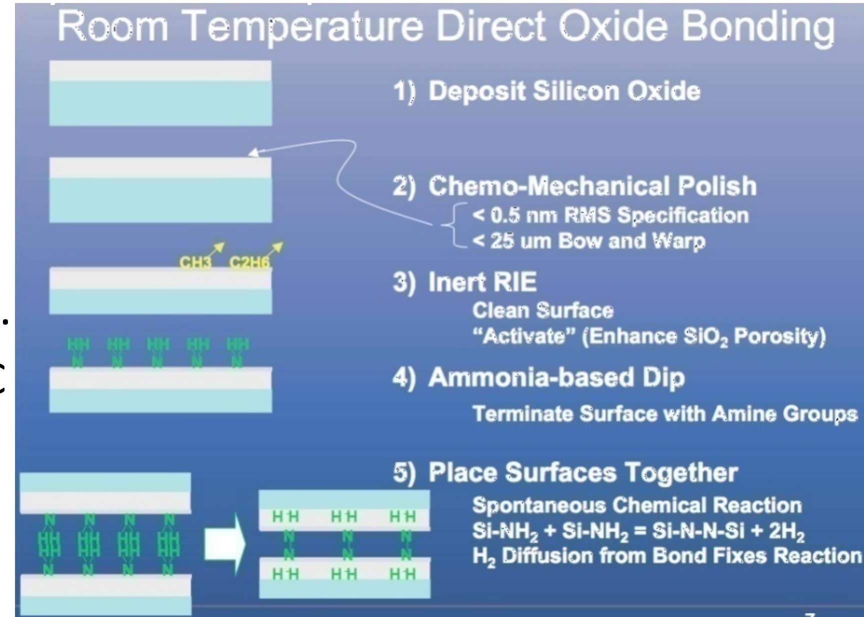
- **3D IC vendors with commercially available bonding process**
  - Tezzaron – Cu-Cu thermo-compression for bonding
  - Zycube – Adhesive and In-Au bump for bonding
  - **Ziptronix - Direct Bond Interconnect based on oxide bonding**

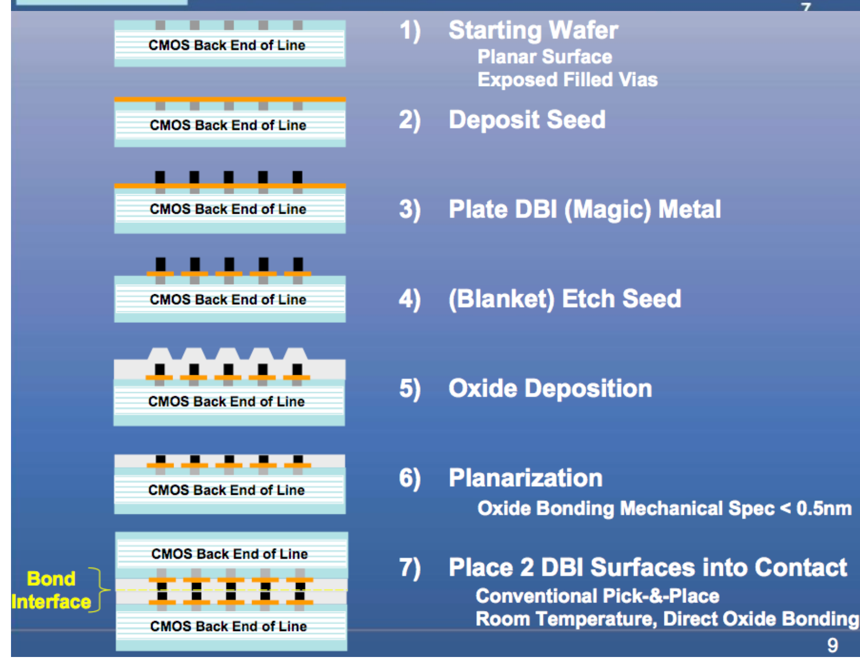
- **Fermilab has worked with Ziptronix to demonstrate the DBI technology for particle physics sensor/ROIC integration.**

DBI Technology

- Oxide bonding at room temperature.
- Metal connection by thermo-compression.
- Robust mechanical connection – sensor/IC can be ground and thinned after bonding.
- 3 µm pitch achieved; also Low mass.
- Die to wafer, wafer to wafer.
- ROICs can be placed onto sensor wafers with 10 µm gaps – pave the way towards thinned full coverage detector planes.
- Could be fairly inexpensive (esp. w2w).







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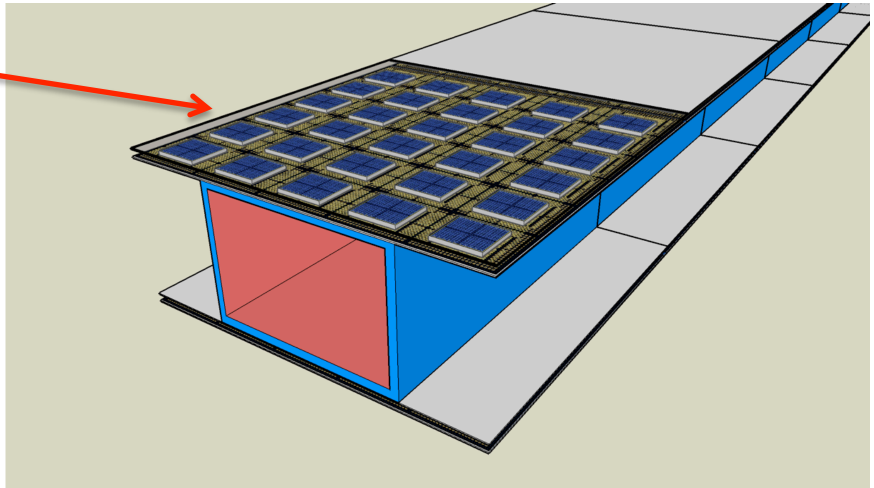
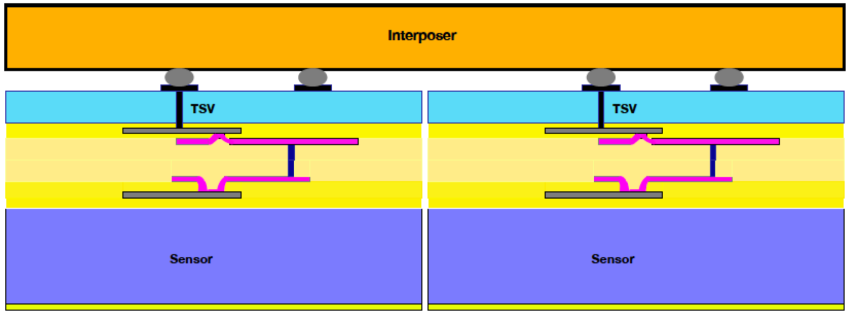
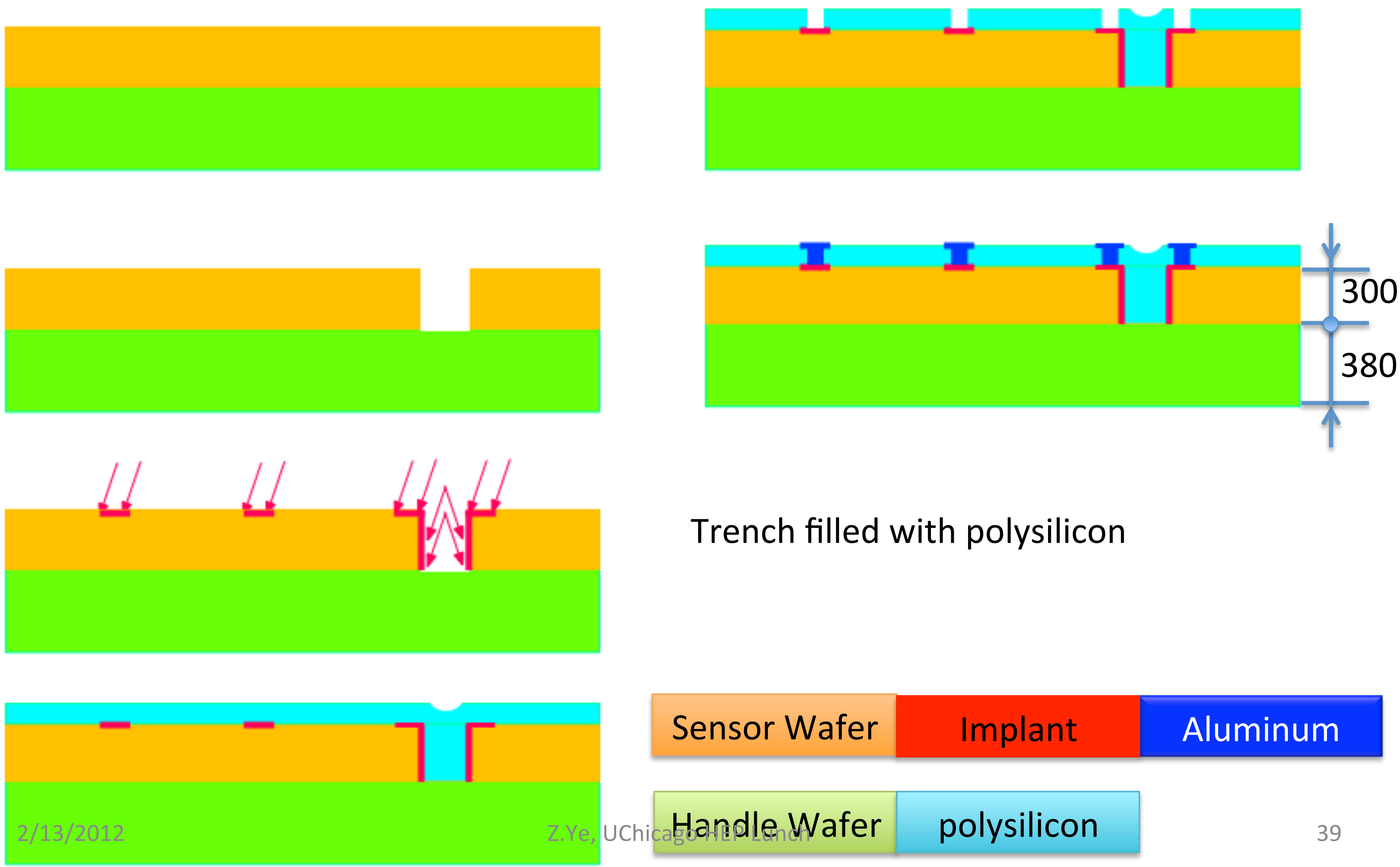
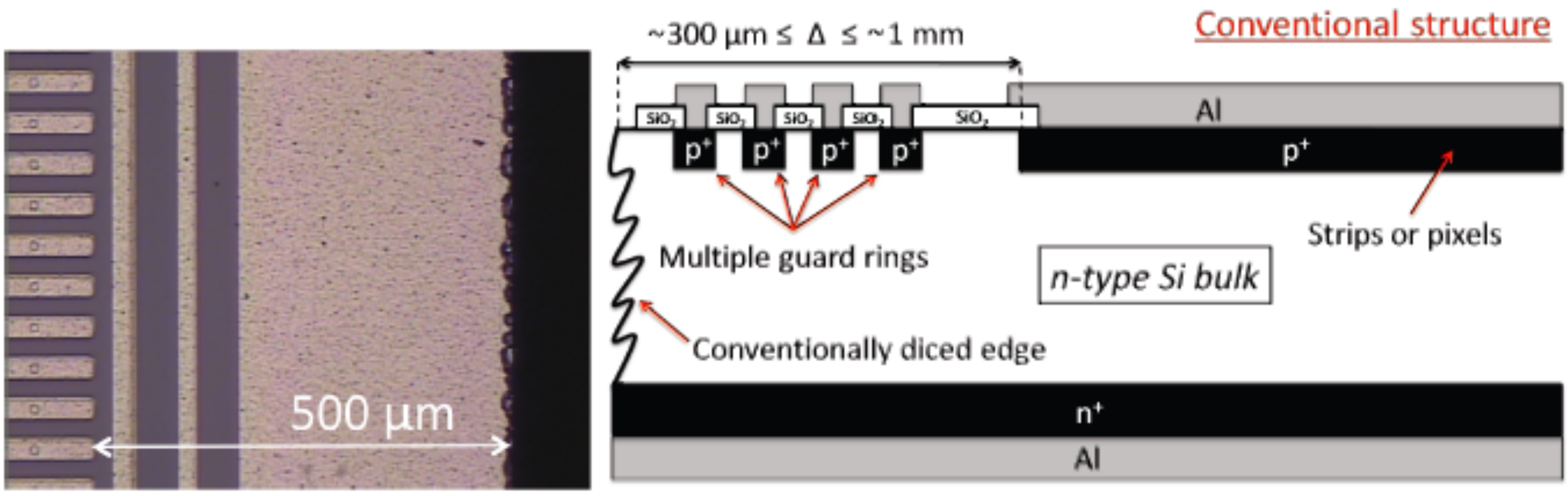


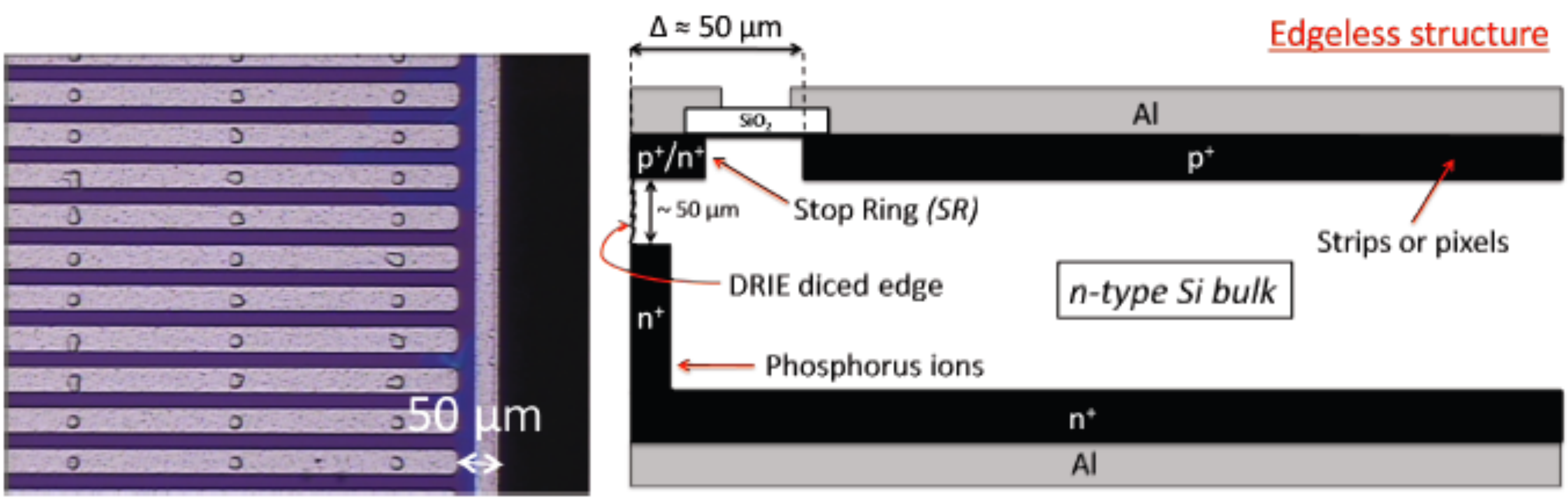


Active Edge Silicon Sensor




500 µm
~300 µm ≤ Δ ≤ ~1 mm
Conventional structure
SiO2
Al
p+
Multiple guard rings
Strips or pixels
n-type Si bulk
Conventionally diced edge
n+
Al

(a)

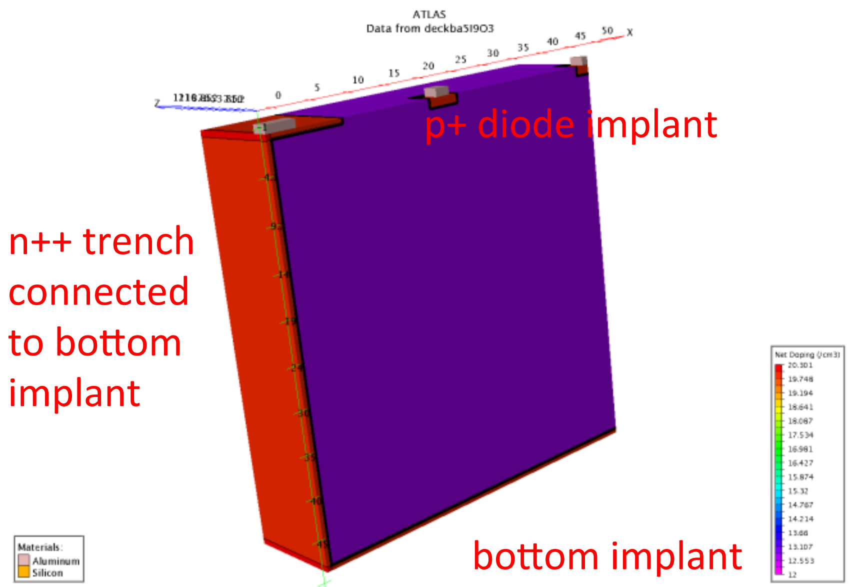

50 µm
Δ ≈ 50 µm
Edgeless structure
SiO2
Al
p+/n+
p+
~ 50 µm
Stop Ring (SR)
Strips or pixels
DRIE diced edge
n-type Si bulk
n+
Phosphorus ions
n+
Al

(b)

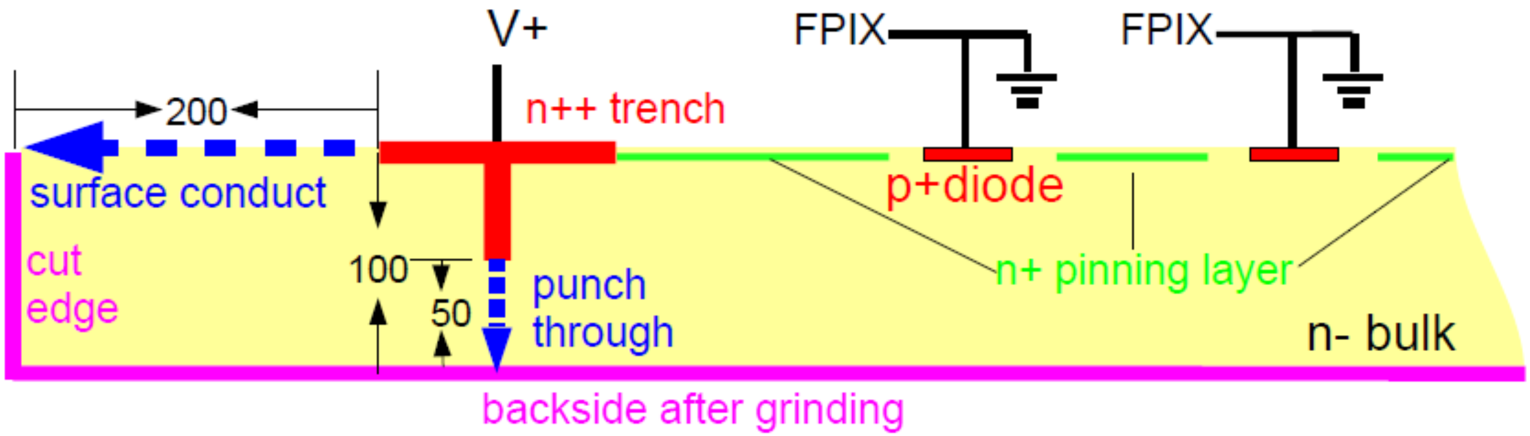
Active Edge Silicon Sensor

- p+ diodes on n- bulk (ρ=5kΩ·cm);
- 22 column x 128 rows
  - 50x600 µm for 1st and 22nd column
  - 50x400 µm for 2nd-21st column
- **50 µm deep n++ trench at the edge**:
  - **can use it as a high quality detector edge;**
  - **can use it as an electrode – eliminating edge losses in tiling reticle-sized detectors.**
- masks designed at Fermilab;
- fabricated by MIT-Lincoln Lab.

Sensor cross section



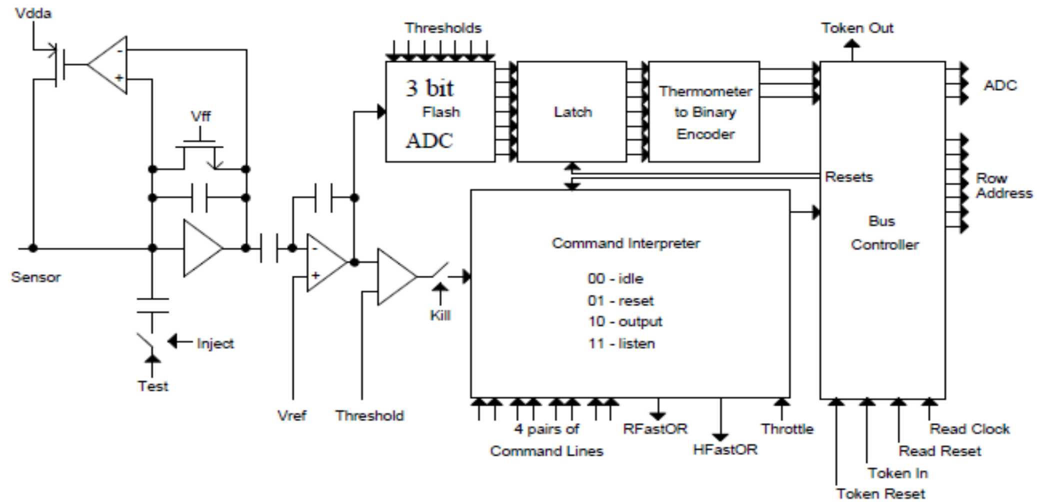
Active Edge Silicon Sensor



- ❑Sensor bias scheme:
  - ➢ p+ diodes (DBI) connected to FPIX input at ground potential;
  - ➢ n++ trench (DBI) connected to positive potential through FPIX.
- ❑The electrical connection from the trench to the ground surface of the backside might be either (a) along the surface and cut edge or (b) by punch-through 50 μm bulk.
- ❑(optional) n+ pinning layer surrounding p+ diodes and extended to trench:
  - ➢commonly used in optical devices to passivate the detector surface;
  - ➢could act as a shield between the detector and ROIC.

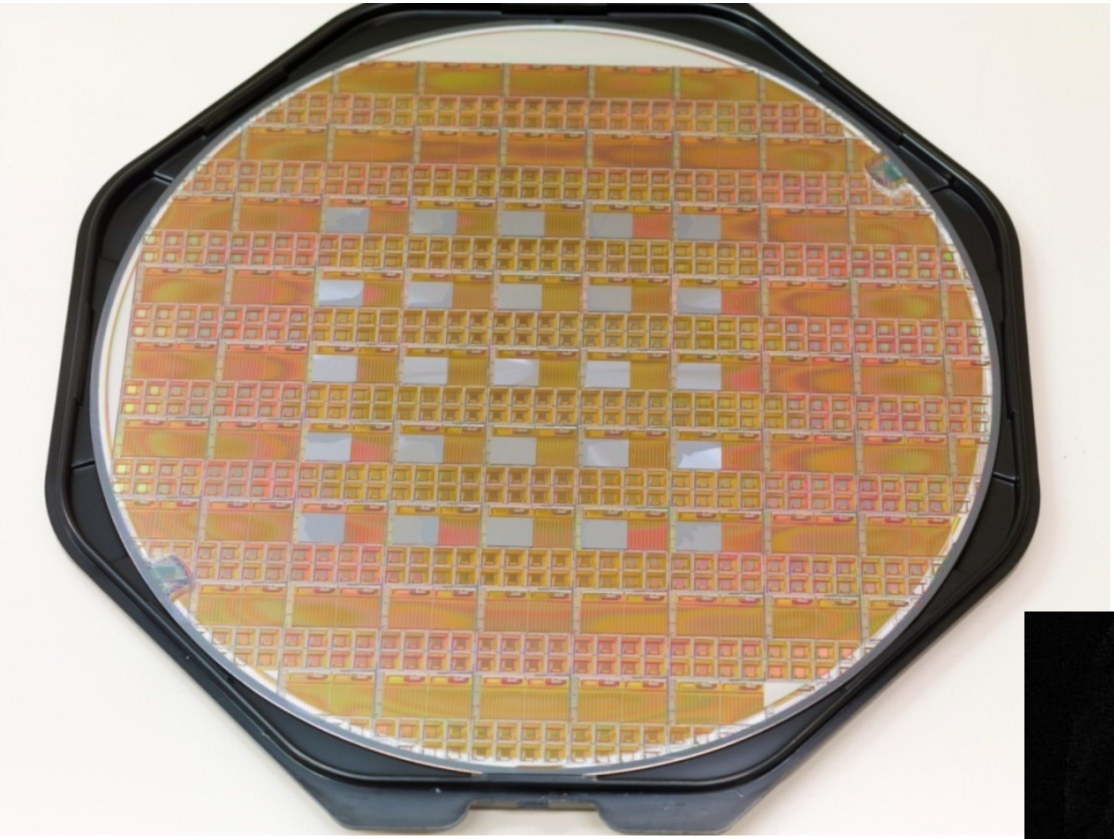
DBI Prototypes

- **Active edge pixel sensor:**
  - p+ diodes on n- bulk (ρ=5kΩ·cm);
  - 22 column x 128 rows
  - 50 µm deep n++ trench at the edge
  - masks designed at Fermilab;
  - fabricated by MIT-Lincoln Lab.
- **BTeV FPIX2.1 readout chip:**
  - 22x128 (C*R) pixel cells of 50x400 µm;
  - designed for e- signals (3 bits ADC), can work with small hole signals but Y/N only;
  - can inject test pulse to capacitor(~3.5fF);
  - debugging pads available for analog and digital output of the pixels in the last row.



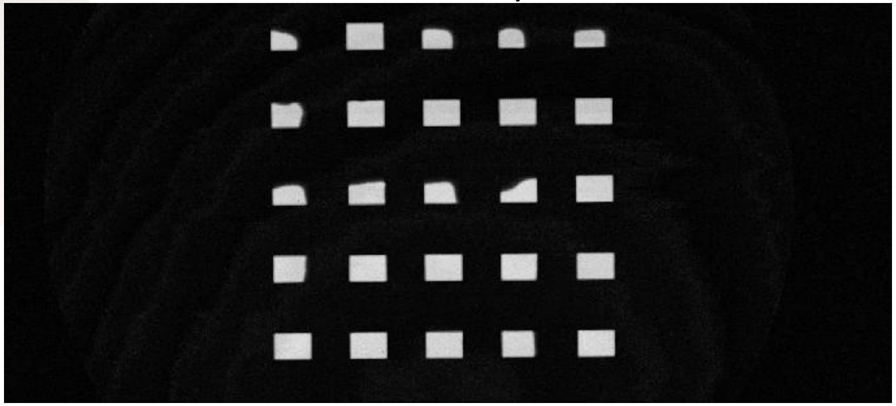
A FPIX2 Pixel Unit Cell

DBI Prototypes



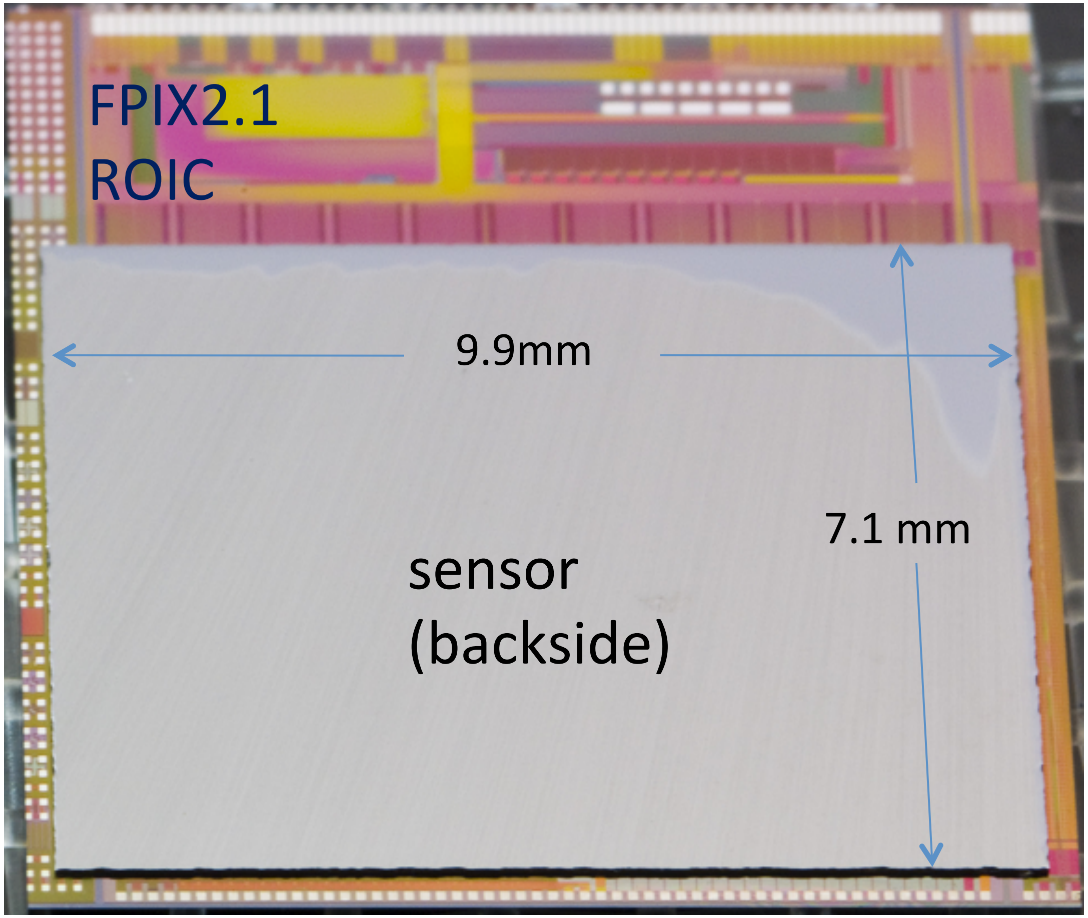
A DBI bonded FPIX wafer by Ziptronix

- 50 MIT_LL sensors DBI bonded to two FPIX wafers by Ziptronix.
- Sensors thinned to 100 µm after bonding, backside not implanted.
- 30 good devices at the end (16 with bond voids indicated by SAM. Normal yield is 80-90% if not dealing with a small number of wafers as us).



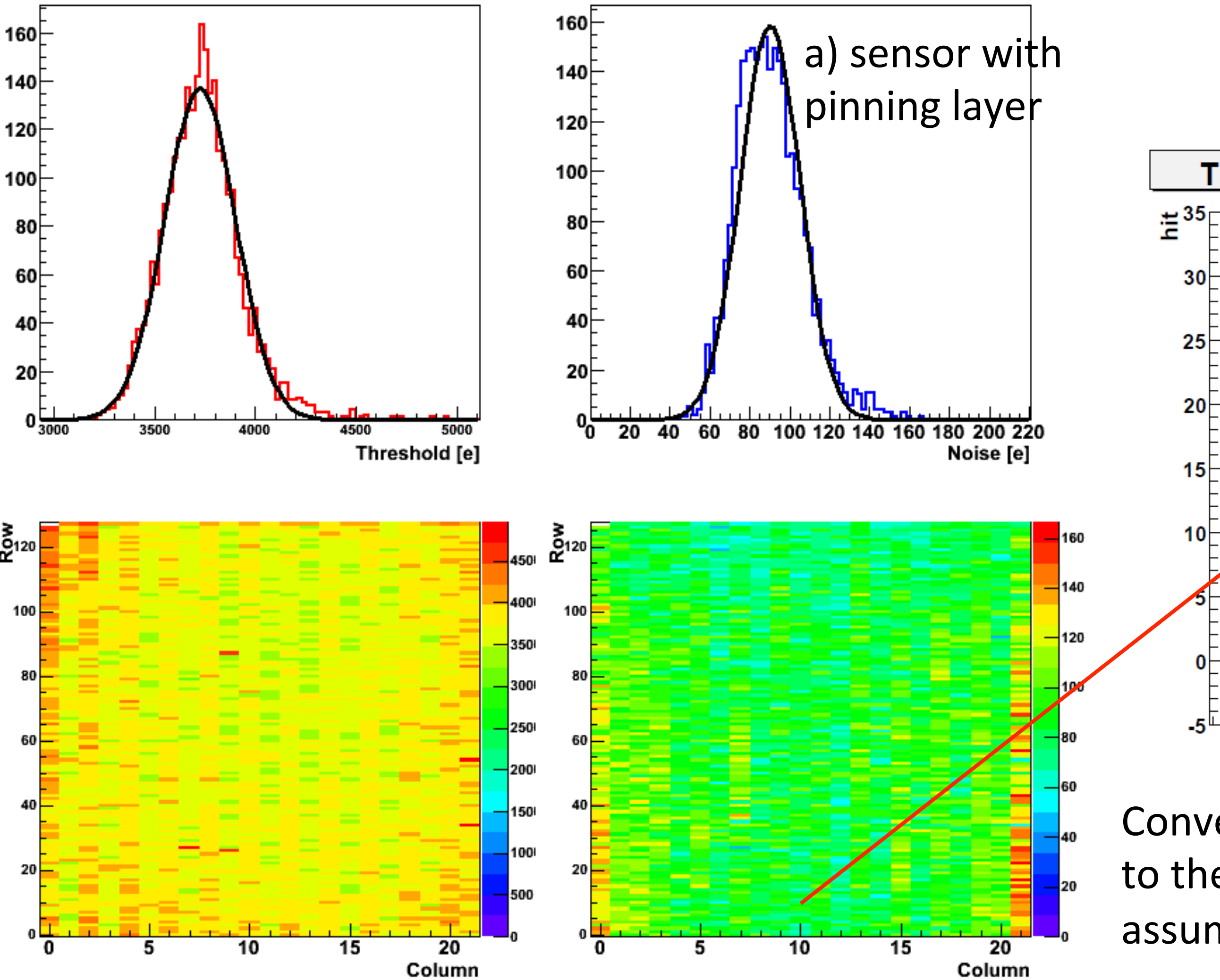
Scanning Acoustic Microscopy

DBI Prototypes

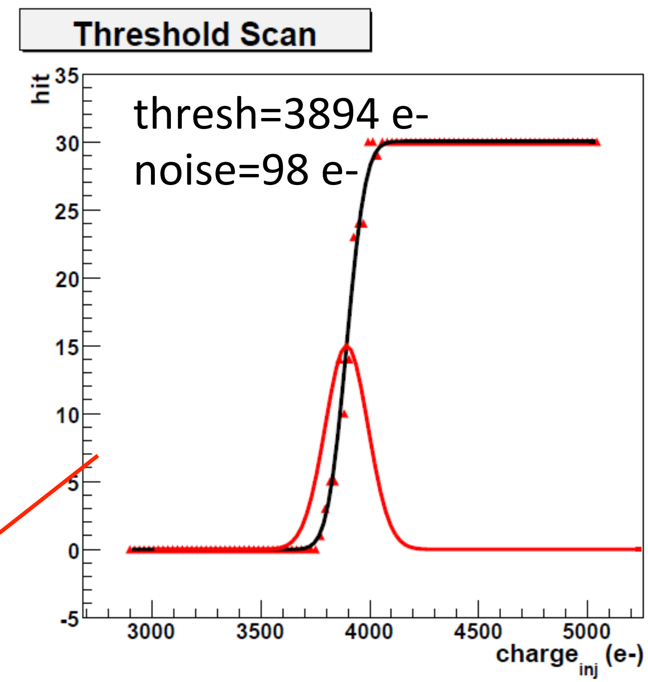


A integrated device after dicing

Threshold Scan

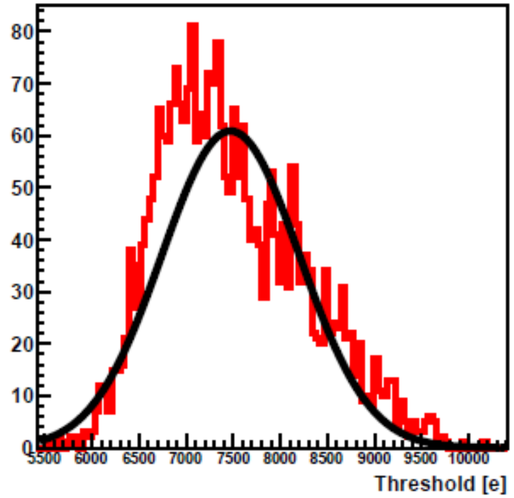


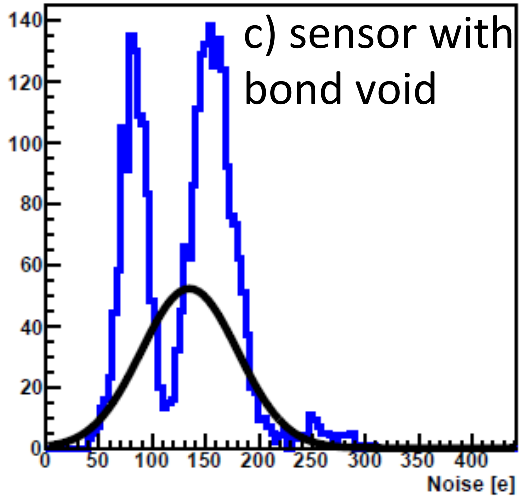
S-curve for pixel (10,10)

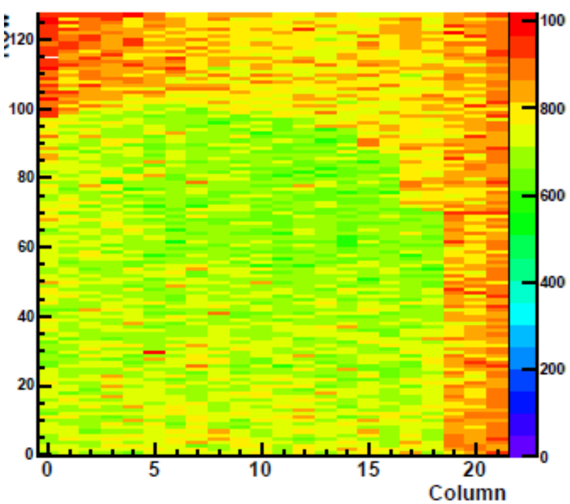


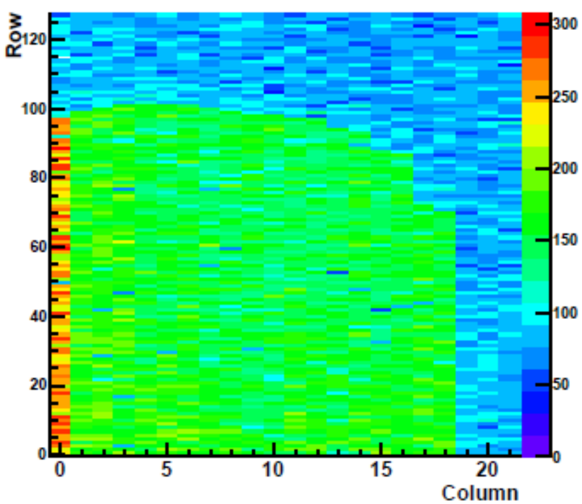
Conversion from the test pulse size to the number of electrons done assuming 3.5fF injection capacitors.

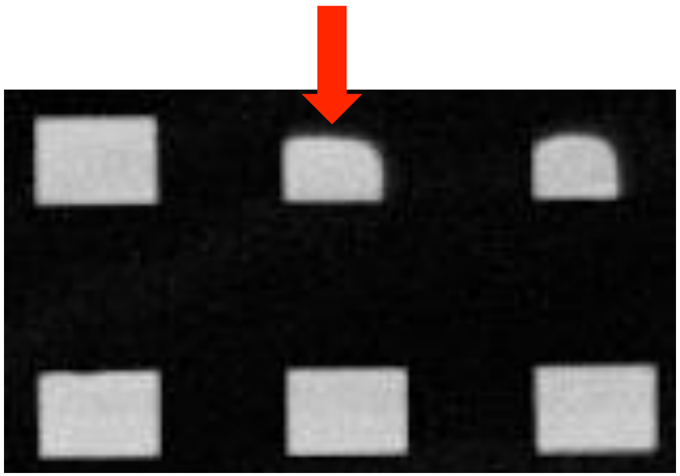
Sensor with Bond Void





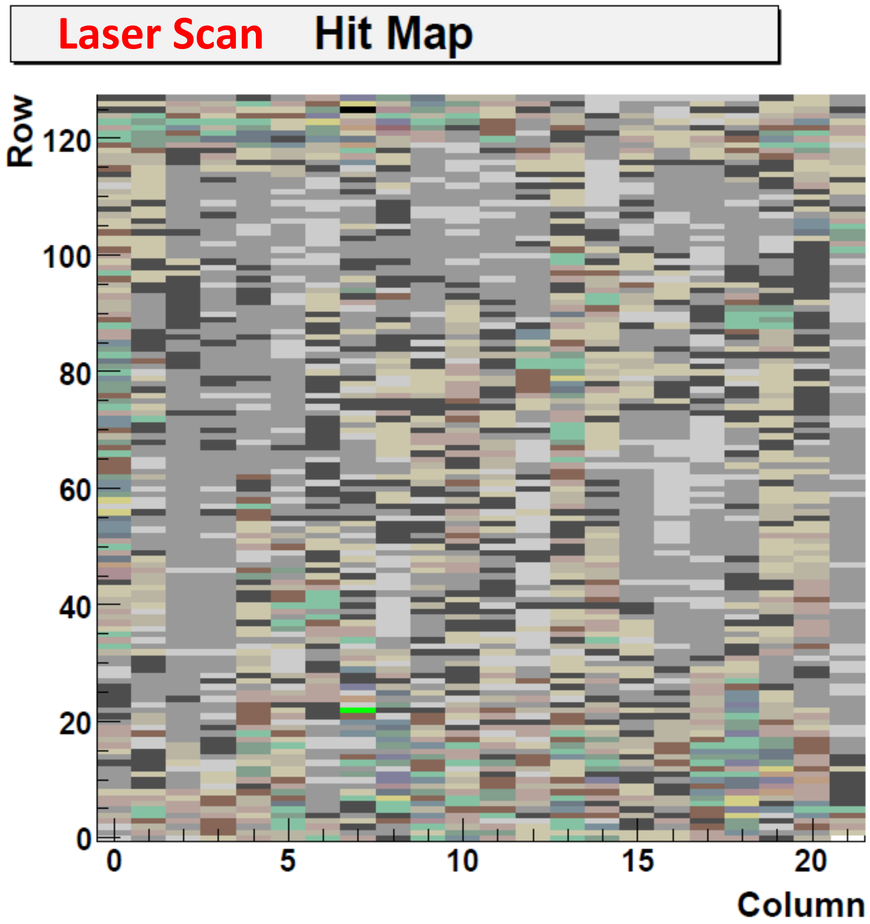


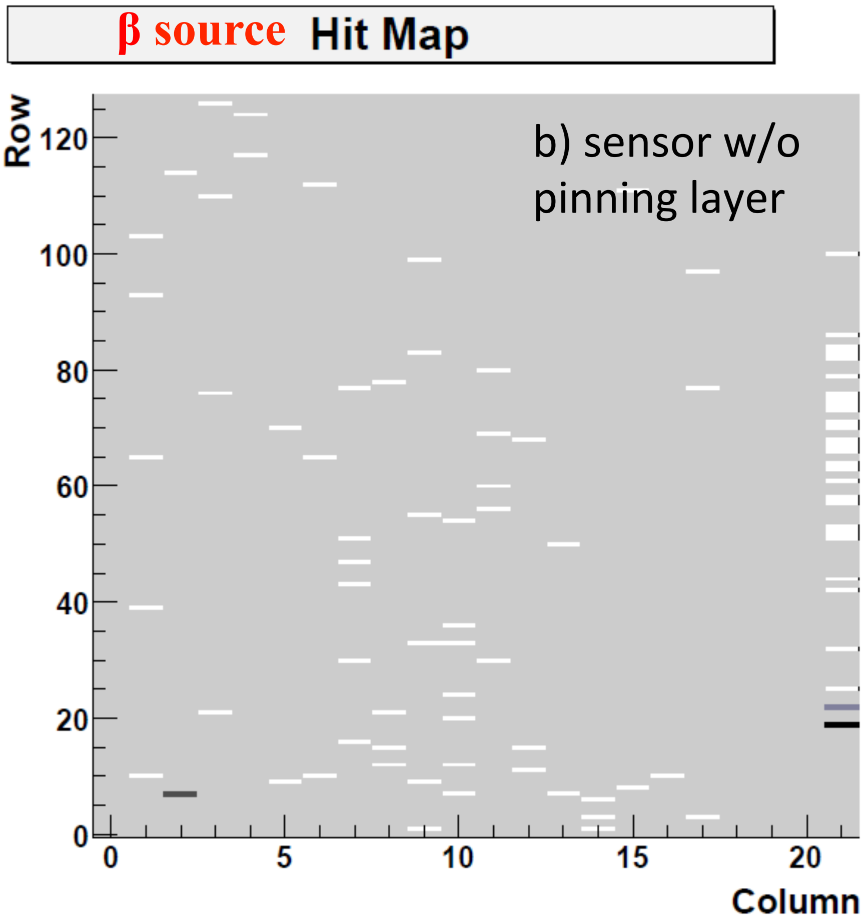




Scanning Acoustic Microscopy

Laser and β Source

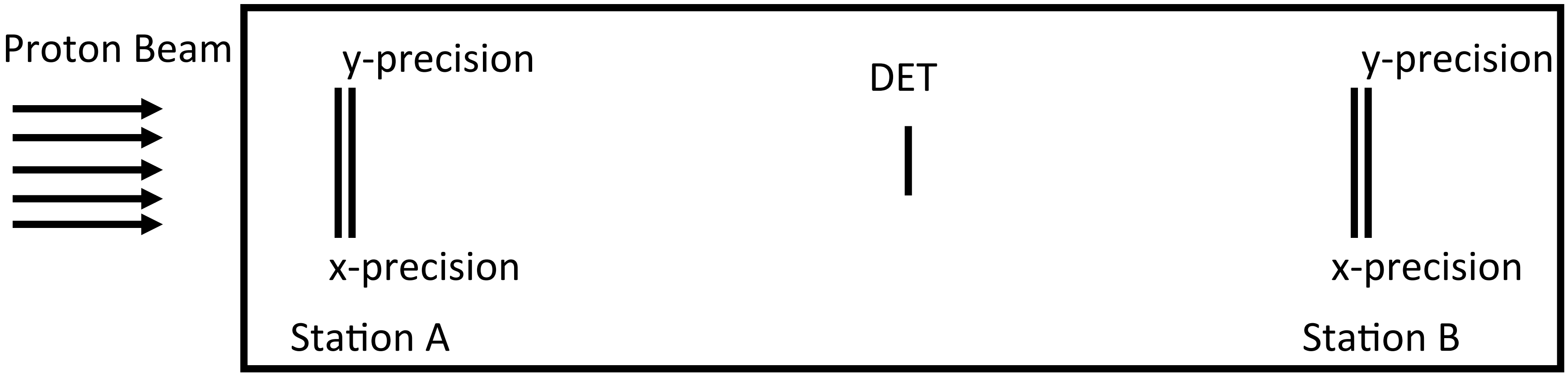




We are able to see the digital outputs of >99% of the channels due to the laser and due to a β source (Sr-90).

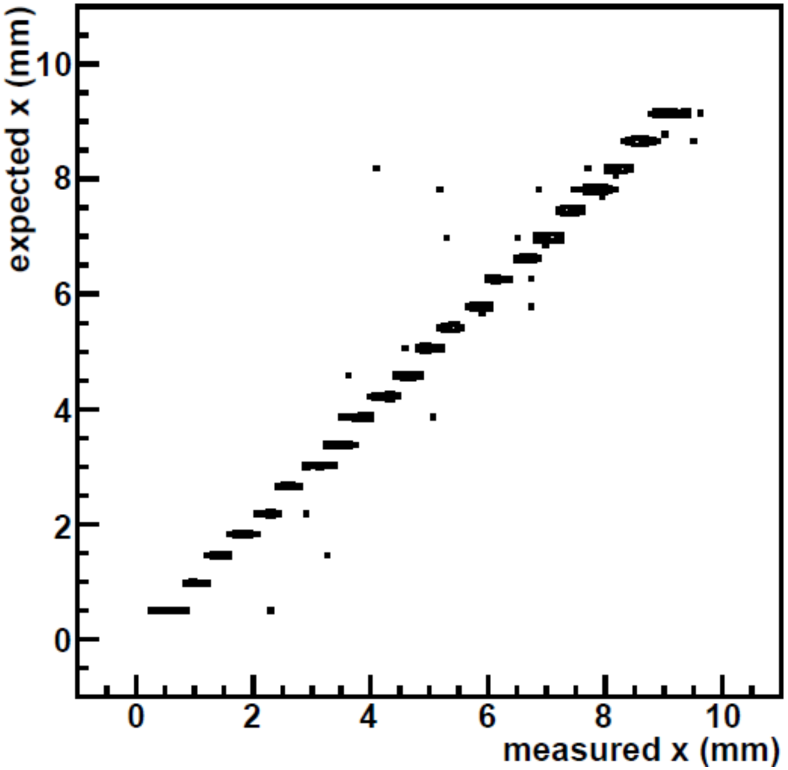
Test Beam Test

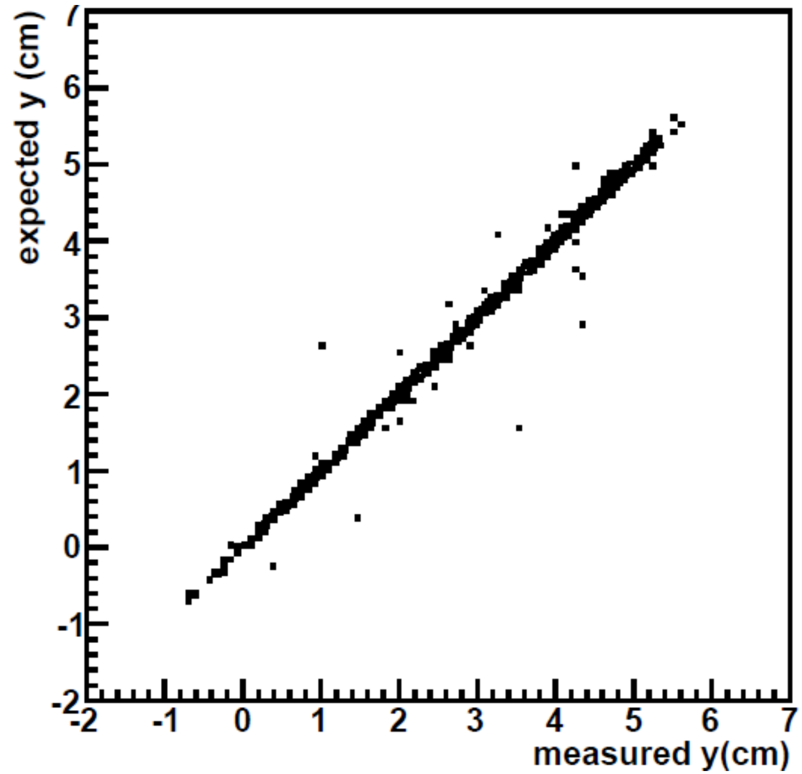
- Fermilab Meson Test Beam Facility 120 GeV proton beam perpendicular to the telescope and DET.
- Two telescope stations of BTeV pixel sensors, with one bit of digital output ("hit") from each 50x400μm pixel unit.



- X/Y positions of the reconstructed hits are "semi-discrete".

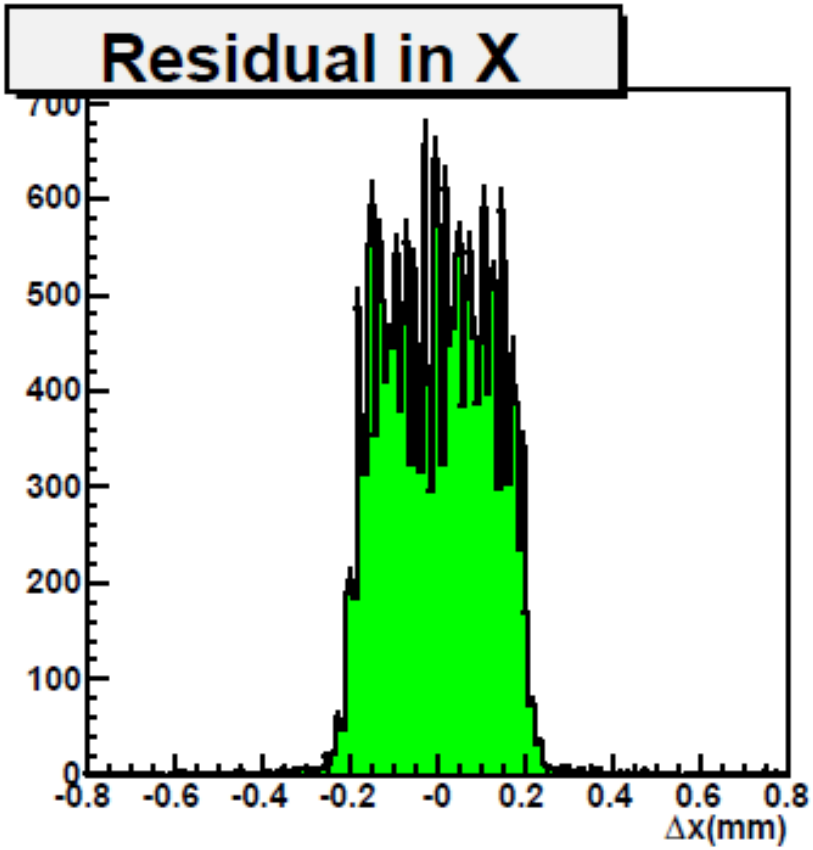
Test Beam Test

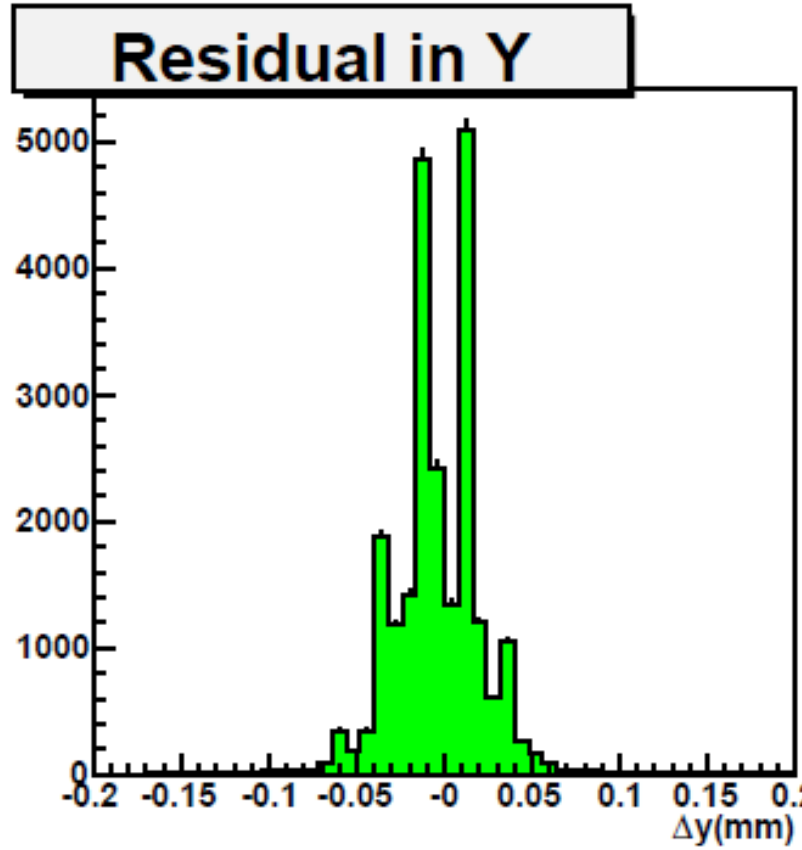




Test Beam Test

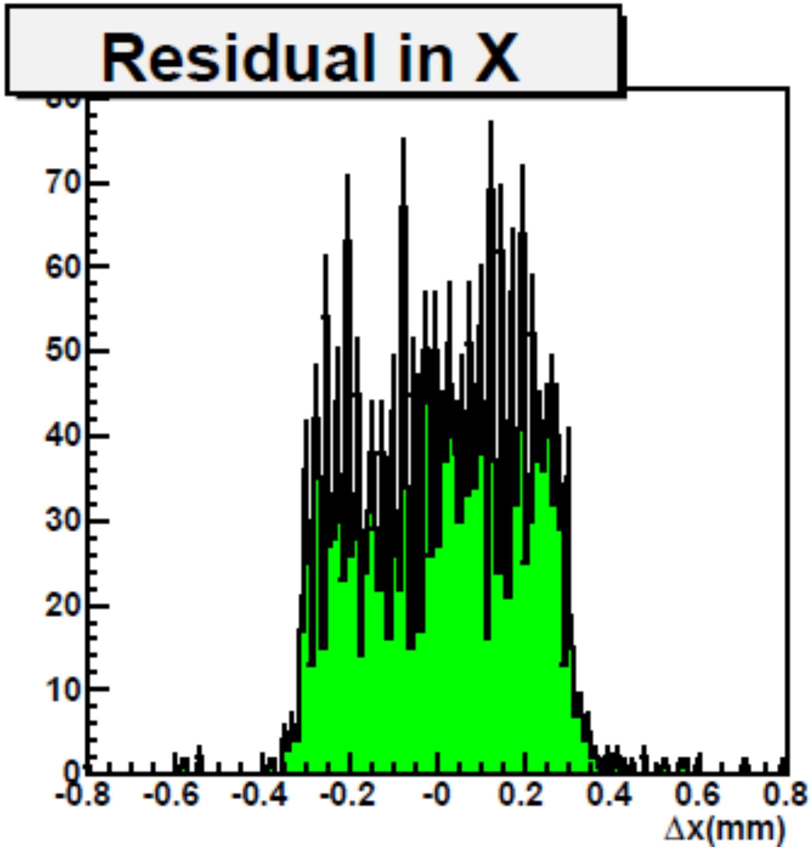
Column 2nd-21st : 400 x 50 μm

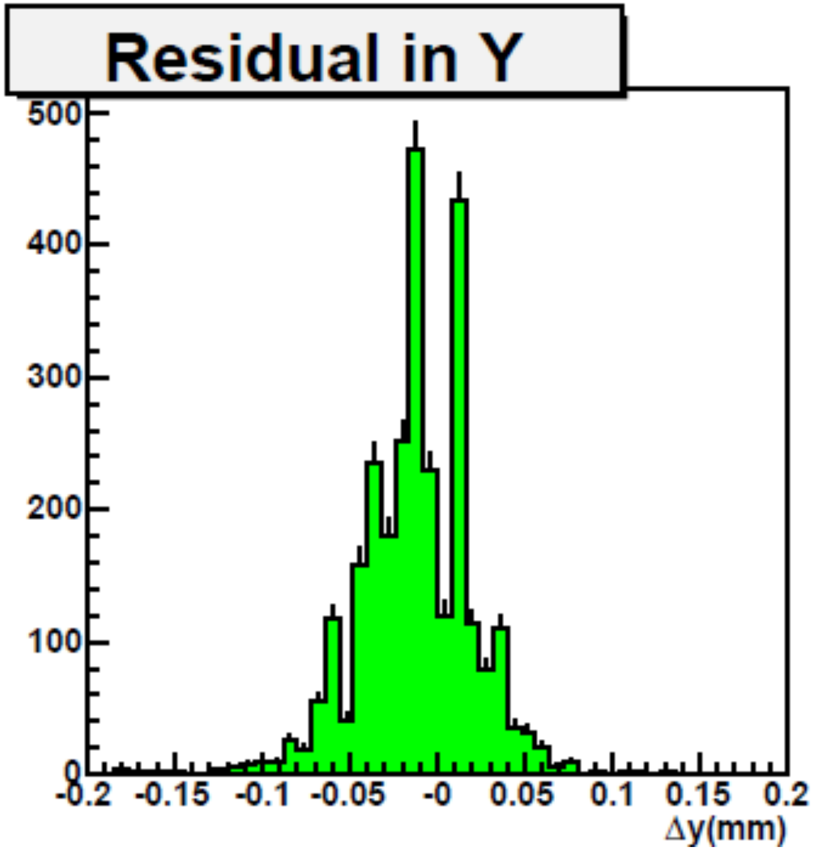




Test Beam Test

Column 1st and 22nd : 600 x 50 μm





Summary and Outlook

- Work towards a proof of concept for a L1 Tracker Trigger for SLHC upgrade with vertical integration techniques.
- A prototype frontend ASIC has been designed and fabricated, and is currently being tested.
- Initial tests suggests that 3D techniques needed for a tracker trigger ASIC are basically working. More studies are underway.
- Some issues discovered with the first prototype chip design and fabrication. Will be considered for the next chip design.

Summary and Outlook

- The DBI technology as a replacement of bump-bonding for particle physics pixel sensor/ROIC integration:
  - Low mass, fine pitch;
  - Sensor/ROIC thinning possible after bonding;
  - Available commercially, fairly inexpensive.
- Tests of DBI bonded devices promising:
  - Active edge pixel sensor mated to FPIX2.1 chip;
  - A very small number of interconnect failures;
  - Sensor input capacitances seem to be small.
  - Radiation damage for DBI bonding done

Plans for 2012-2013

- Test 3D Chip
  - ↓ Integrate with sensor
  - ↓ Bond to stack
  - ↓ Test

- Module Bump bonding
  - ↓ Test assembly
  - ↓ Iterate with interposer II
  - ↓ Test

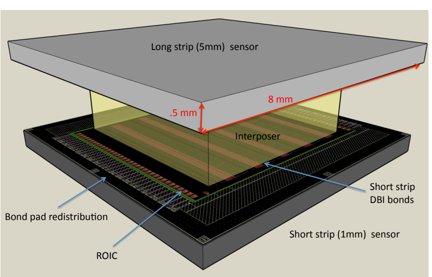
- Design Data flow chip
  - ↓ Fabricate
  - ↓ Test

- Mechanical Design

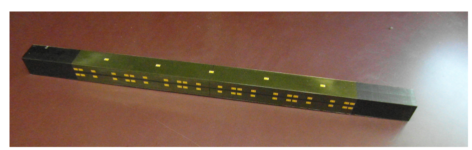
- Active edge sensor design
  - ↓ Sensor Fabrication
  - ↓ Tile Production
  - ↓ Assembly bump bond

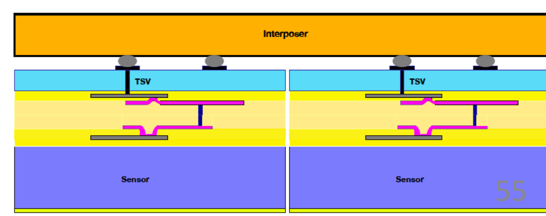
- Interposer + dummy sensor
  - ↓ Fabrication
  - ↓ Assembly bump bond

- Assembly bump bond
  - ↓ Test



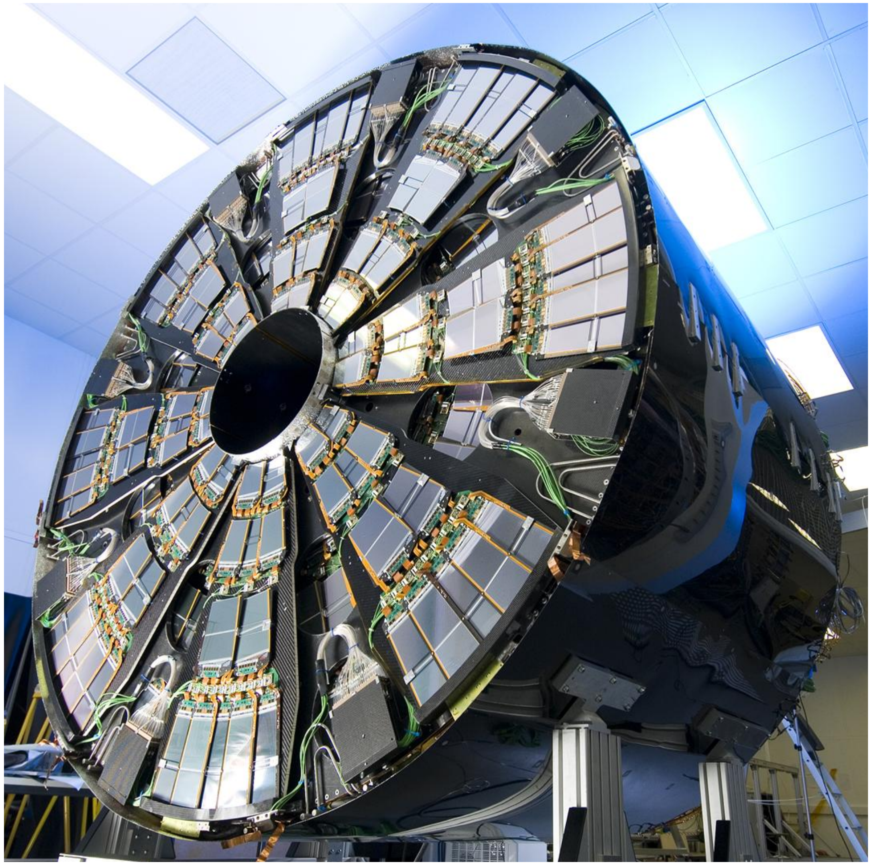
Demonstration Stack

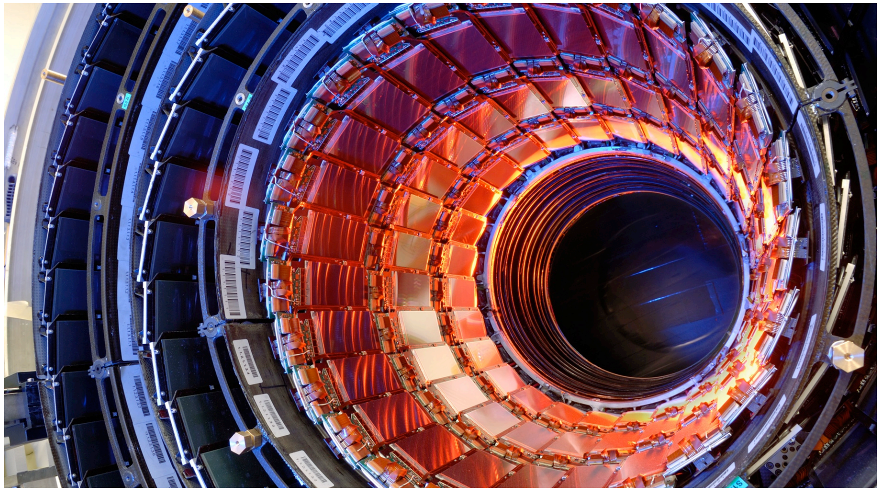




Backup Slides Start Here

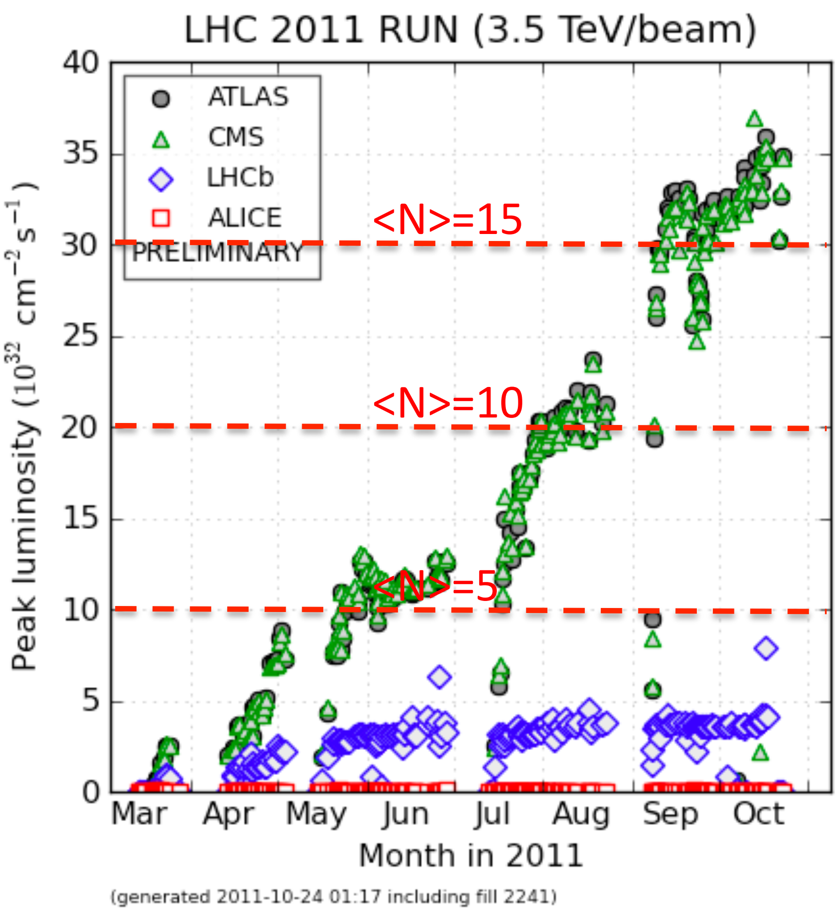
CMS Silicon Tracker

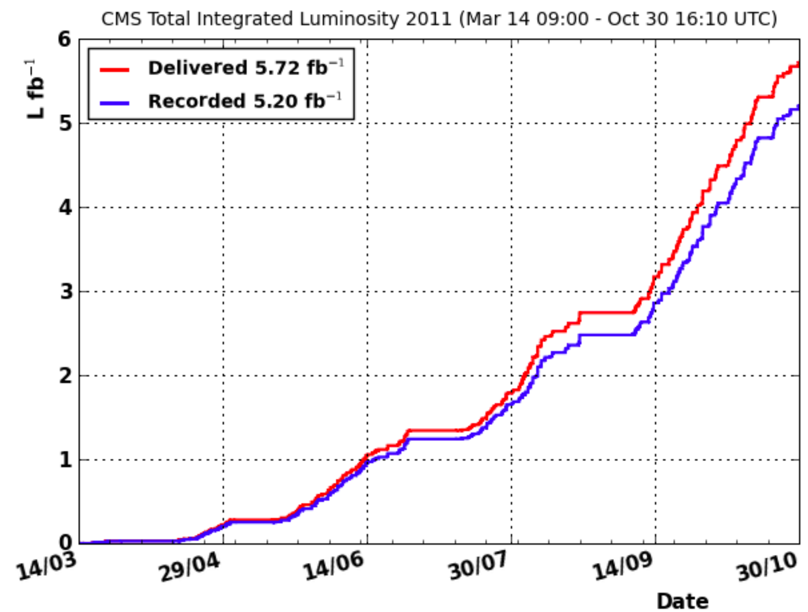




World Largest Silicon Device
200 m^2, >70 million channels
3 layers of pixels, 10 layers of strips

CMS Data Taking



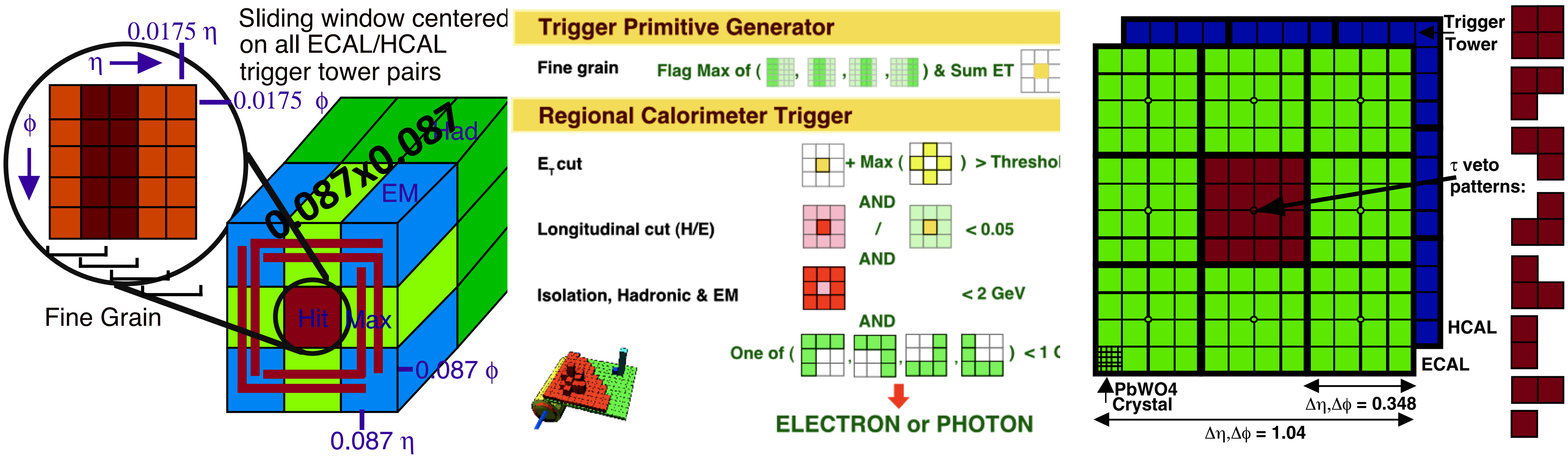


Rapid increase in instantaneous luminosity:

April $L=2.0\times10^{32}\ cm^{-2}s^{-1}$

October $L=3.5\times10^{33}\ cm^{-2}s^{-1}$

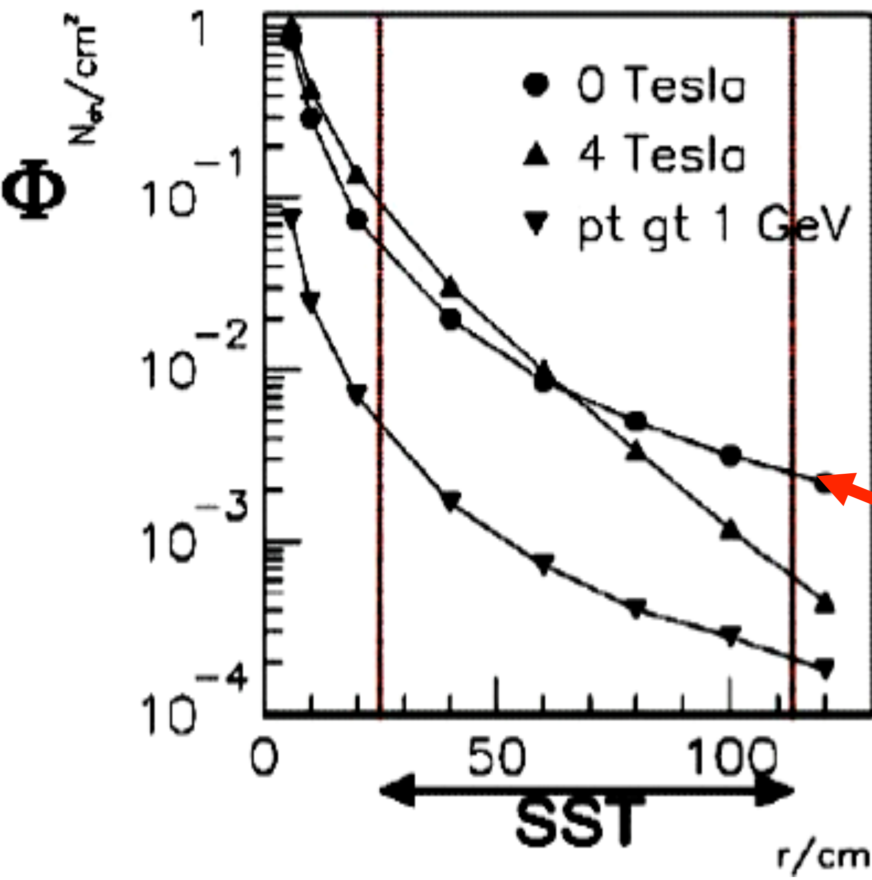
The Lv1 Algorithms



- **Electron/Photon triggers:**
  - Electron (Hit Tower + Max)
    - 2-tower ΣET + Hit tower H/E
    - Hit tower 2x5-crystal strips >90% ET in 5x5 (Fine Grain)
  - Isolated Electron (3x3 Tower)
    - Quiet neighbors: all towers pass Fine Grain & H/E
    - One group of 5 EM ET < Thr.
- **Forward Central and Tau Jet Triggers**
  - Search for E_t bumps within 12x12 Trigger Tower (TT) window (1 TT= 0.087x0.087)
  - Sort in E_t and transmit the 4 highest E_t jets + position information to the Global Trigger.
  - Tau-Jets are central jets which have tau-Veto off (collimation cut)

The Challenges at SLHC

Number of Charged Particles/bx/cm²



At SLHC we expect:

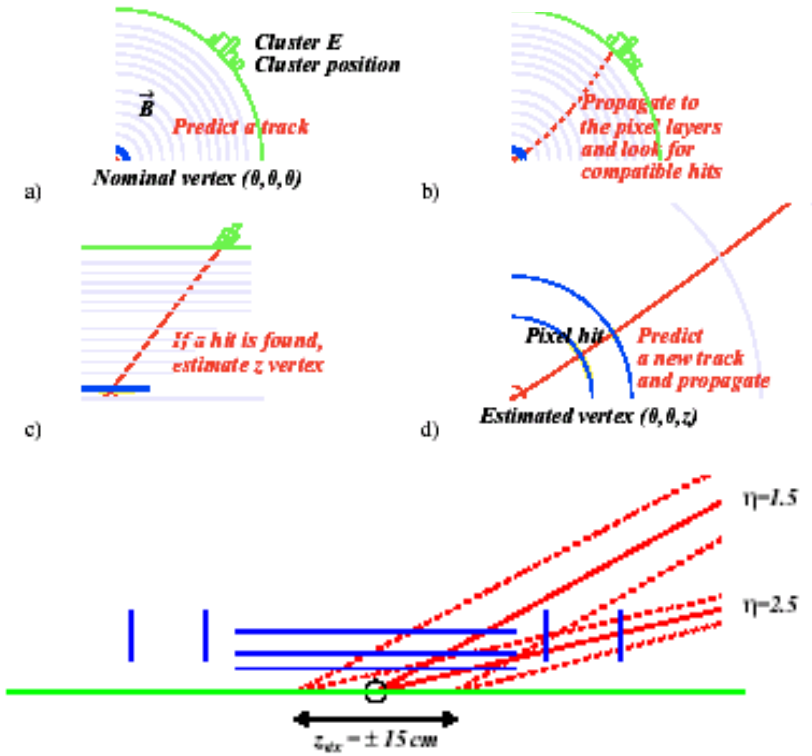
Occupancy (10^{35} hits/cm² /25 nsec)
17.6 at R=4 cm
7.6 at R=7 cm
4.6 at R=10 cm

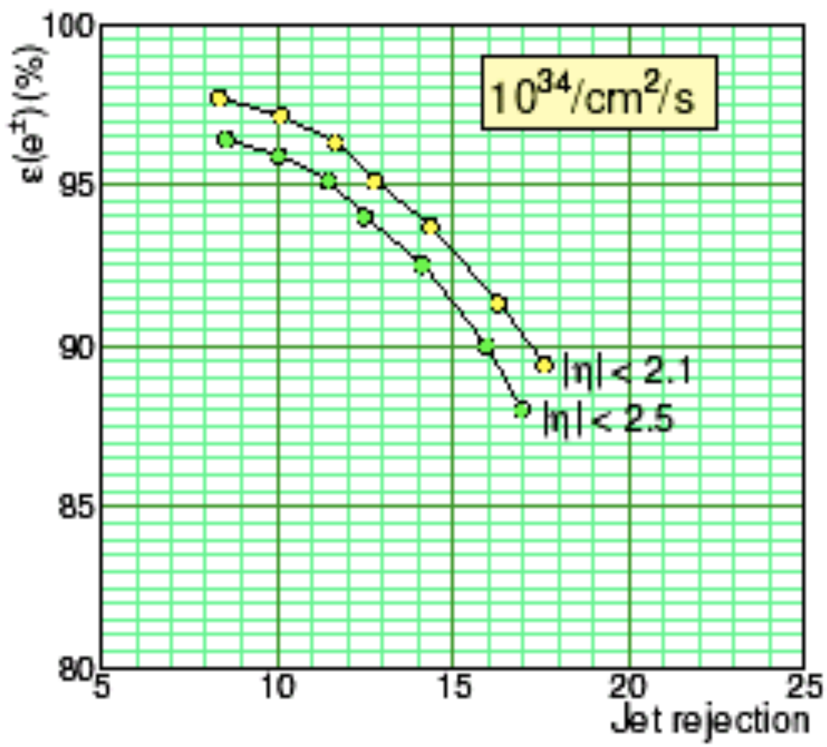
- **The rate is dominated by particles with momentum below 1 GeV.**
- **These move helix-trajectories around the beam axis.**

- Expected data rates from the Inner tracker are very large resulting to ~10^1 TBytes/sec/cm²
- This rate needs to be reduced on the detector.
- 90% of the rate comes from particles below 1 GeV in Pt

Using Tracking Information for Triggering

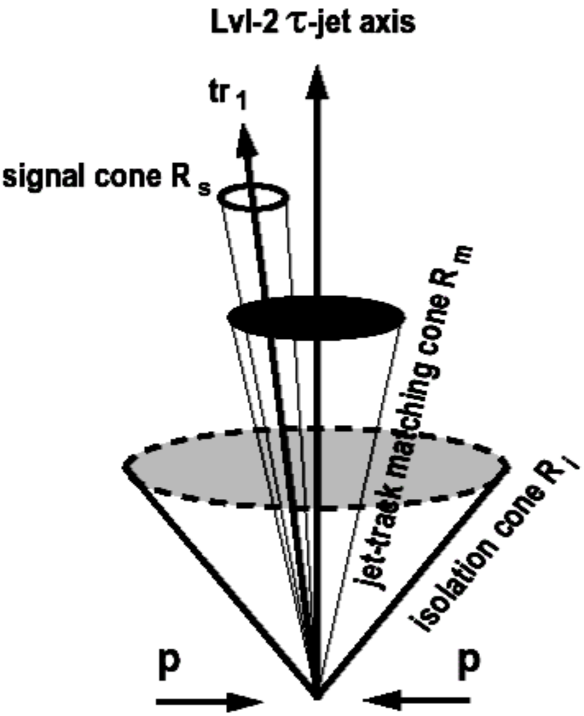
Electron/Photon Triggers



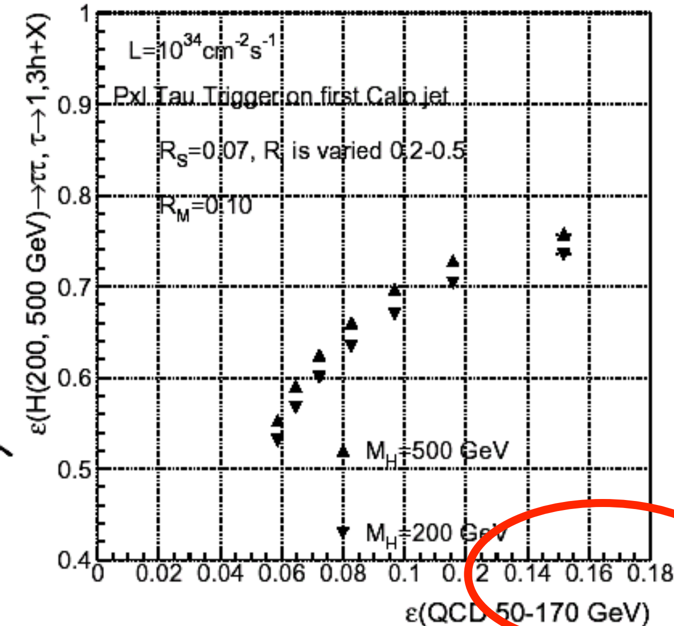


- Electron Triggers:
  - A factor of 10 reduction using hits in the pixels
  - A factor of 3 using the outer tracker

Using Tracking Information for Triggering



Tau and Muon Triggers with tracking



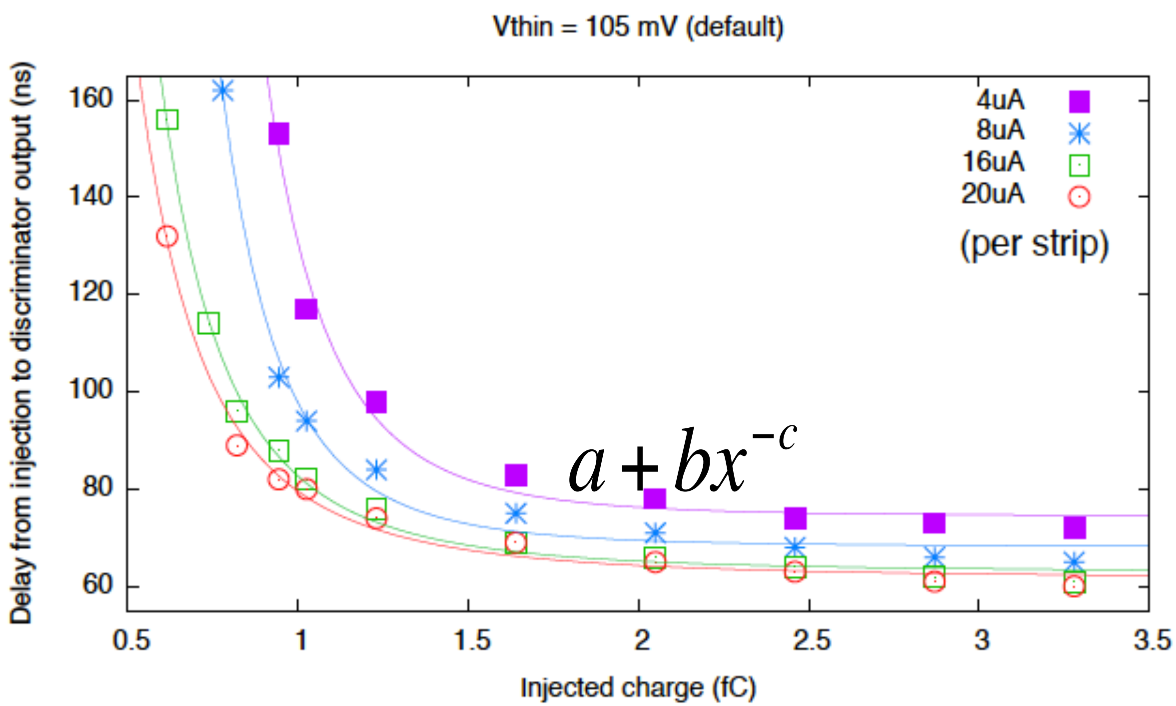
Efficiency for QCD events

Level	Rate (Hz) Single	Double
Level-1	6200	1700
Level-2	700	35
Calo isolation	590	25
Level-3	100	10
Level-3+calo +tracker isolation	50	5
Total	55	

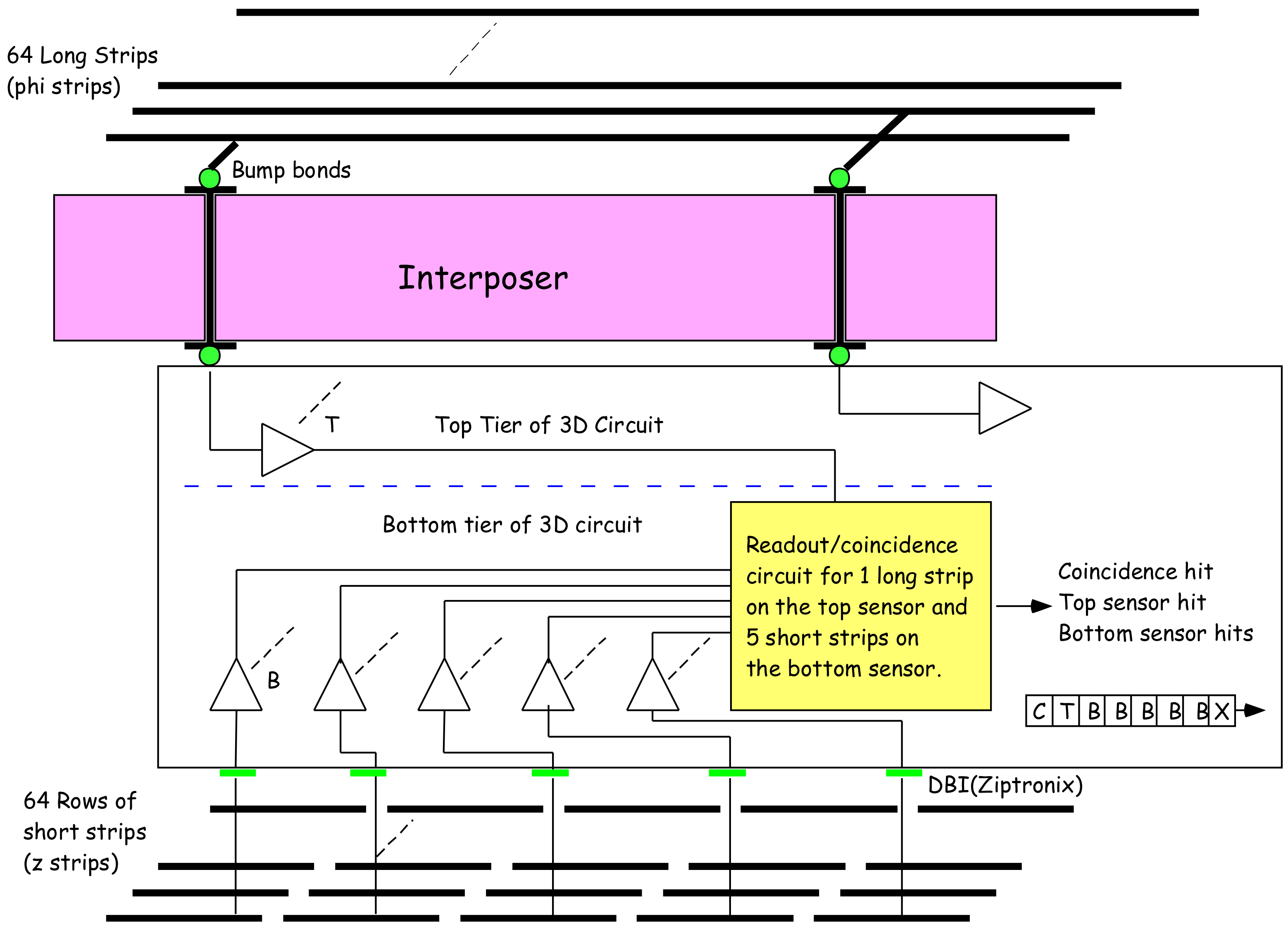
- **Tau Trigger:**
  - Uses isolated stubs in the pixels
  - A factor of 10 in QCD jet rejection
- **Muon Trigger:**
  - Outer tracker
  - Large rejection

2D Short Strip - Time Walk

- Measure the time delay between the charge injection and detection (fast OR) Convert the voltage to amount of charge assuming the design capacitance of the charge injection capacitors
- Vary the preamp bias voltage to adjust the front end bias current



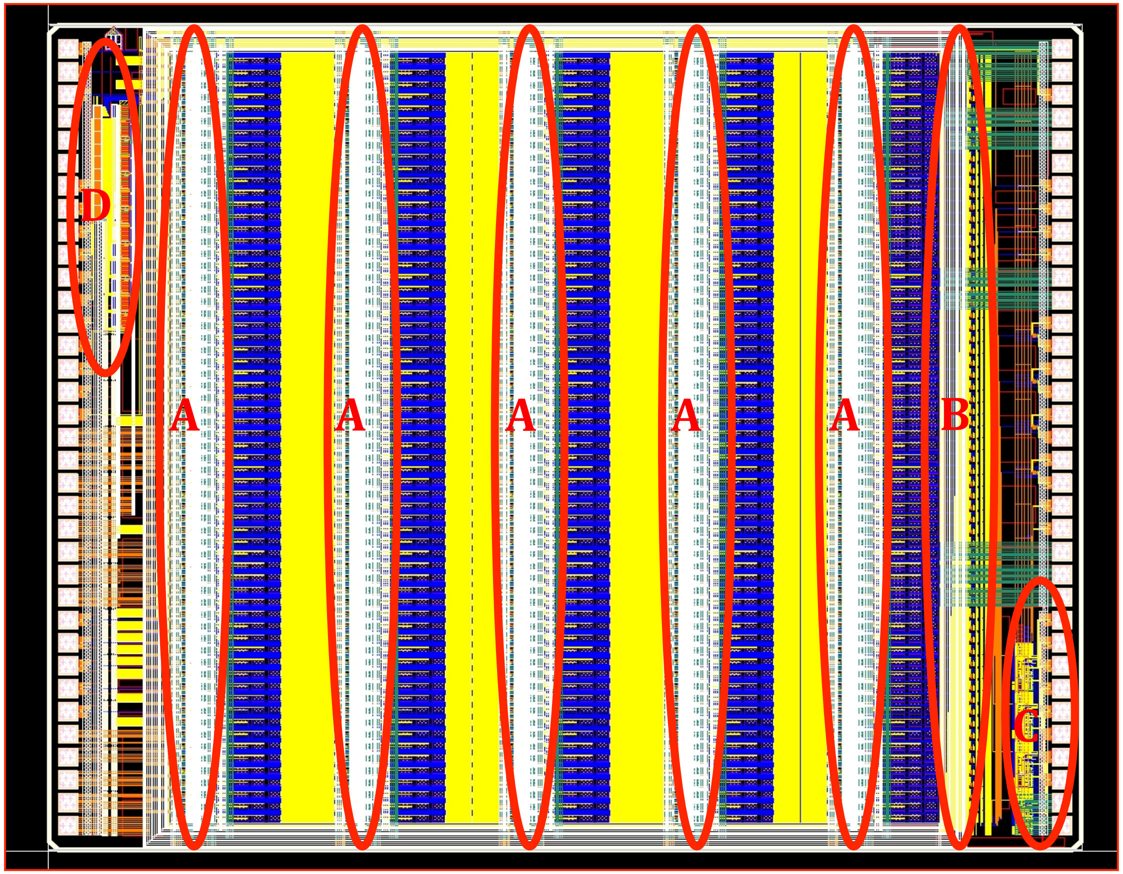
Simplified Functional View of CMS Demonstrator Chip



Why Did 3D Fab Take So Long?

- Design Issues
  - Everyone did not use the same design kit provided by Tezzaron. Some design rules were interpreted incorrectly leading to various TSV design problems.
  - Initially some designs did not use a fill program resulting in fill problems later on
  - The bond pad interface pattern must be uniform across a reticule. Repeated requests to route on the bond layer had to be denied.
  - SRAM cells raised numerous questions.
  - MicroMagic software issues.
- Submission Issues
  - After designs were completed Chartered requested additional street space. It took three submissions before Chartered would finally accept the frame.
  - Individual blocks were incorrectly mirrored by the mask house
  - Chartered would not accept some error waivers we thought were acceptable.
  - Some designs were submitted with incorrect mirroring
- Fabrication Issues
  - 3D fabrication done in Chartered prototype line
  - Chartered was bought by Global Foundries which slowed our wafer fabrication process
  - Global/Chartered did not properly place frames on wafers for 4 different lots of wafers
  - Due to delays in fabrication, the 3D wafer bonding facilities were not available when the wafers were ready.

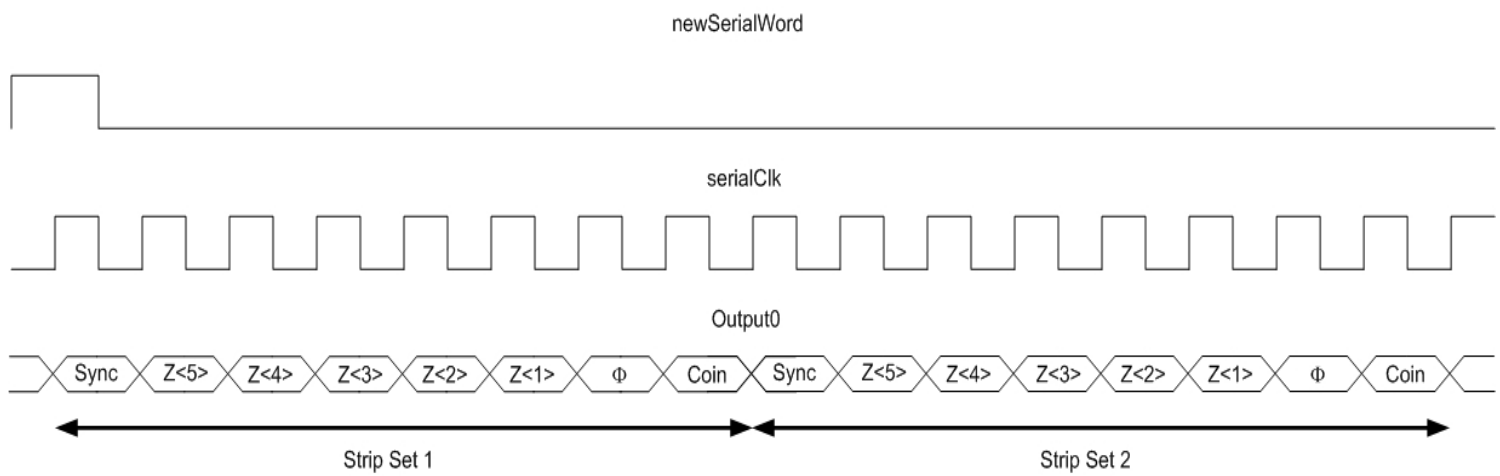
VICTR Layout – Short Strip Tier



A: front-ends for 320 (5x64) strips
B: back-end readout architecture
C: LVDS drivers for readout output
D: DACs providing front-end bias

VICTR Readout Structure

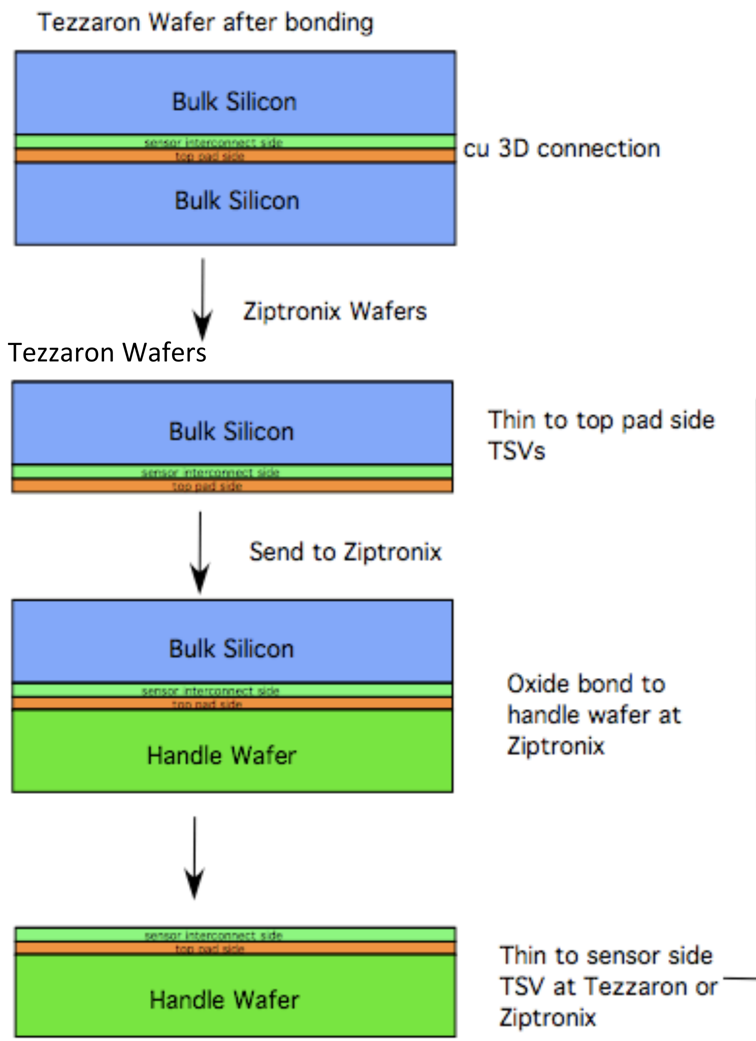
Each strip set contributes 8-bits to the output stream – 1 coincidence bit, 1 long strip (Φ) hit, 5 short strip (Z) hits, and a Sync Bit. These are driven off the chip serially

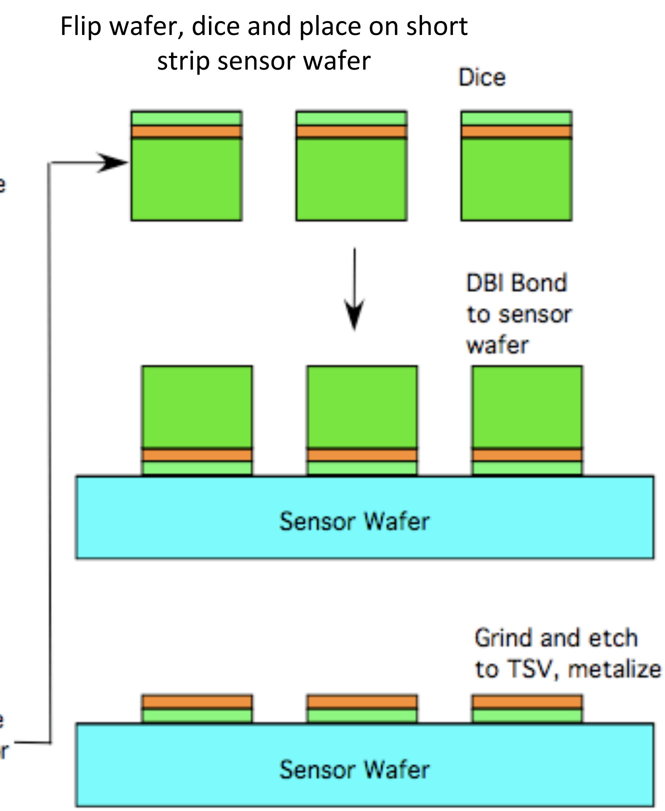


Empty	10000000100000001000000010000000…
Single Φ hit in Strip set 1	10000010100000001000000010000000…
Z<2>-Φ coincident hit in Strip set 2	10000000100000001000101110000000…

How to Build – 3D Integration

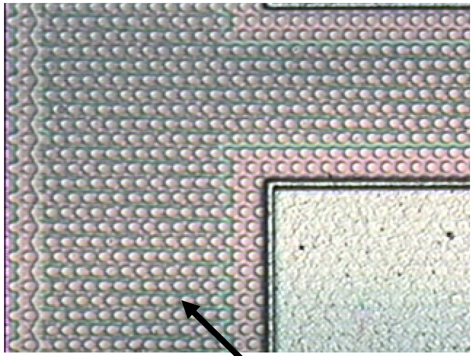
thinning, alignment, oxide bonding, cu-cu bonding, through-silicon-via, …

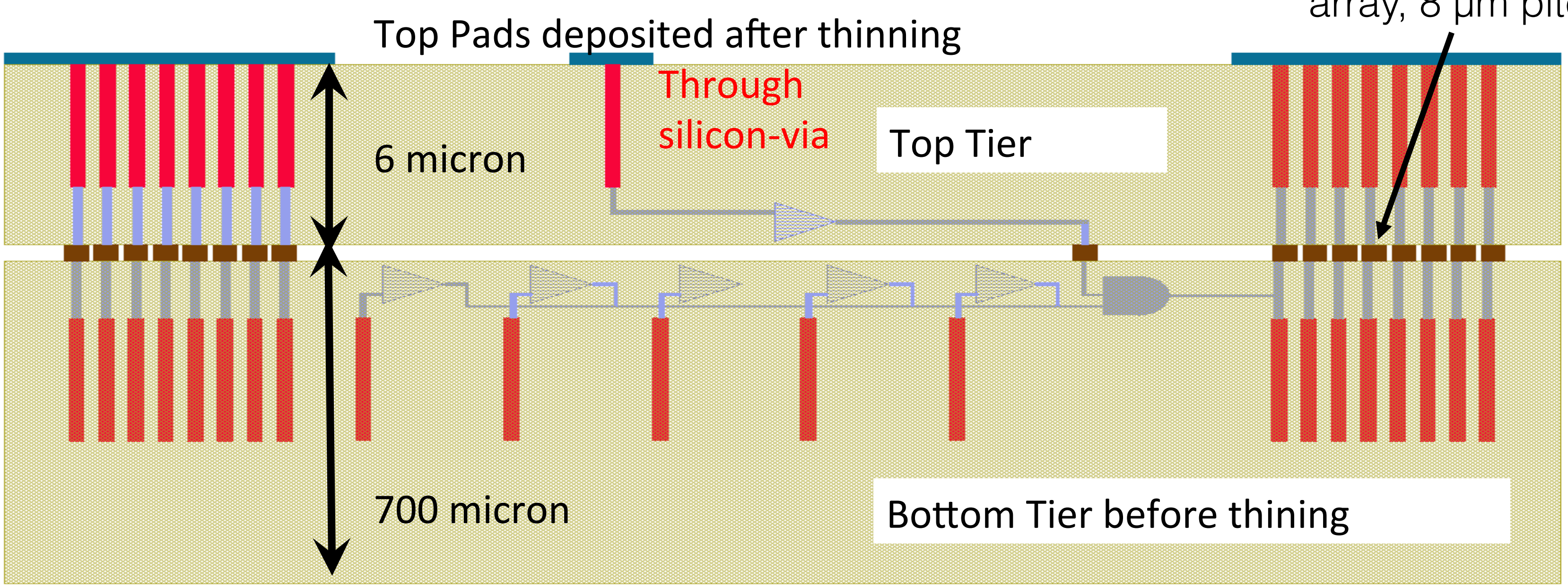




First Prototype ROIC - VICTR

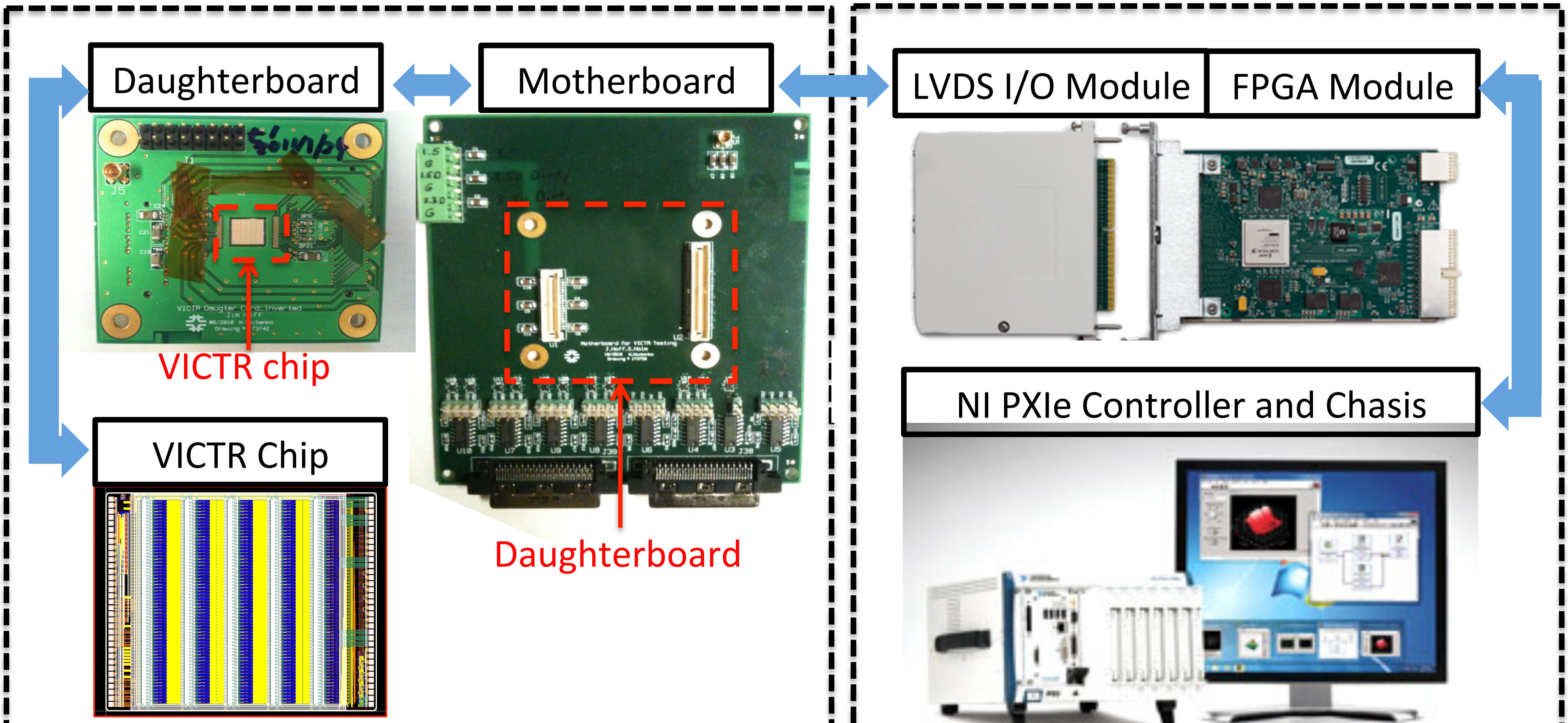
- Two tiers vertically (3D) integrated with Cu-Cu bonding:
  - Frontend signal amplification, shaping and discrimination for top and bottom sensors done separately in the top and bottom tiers.
  - Transfer discriminator output from the top to the bottom tier and form a simple top/bottom coincidence for each set of 1 long top strip and 5 short bottom strips with the same Φ value.
  - Expect considerable increase in complexity as we move towards the final design, such as the incorporation of neighbor hits into the coincidence detection circuitry.

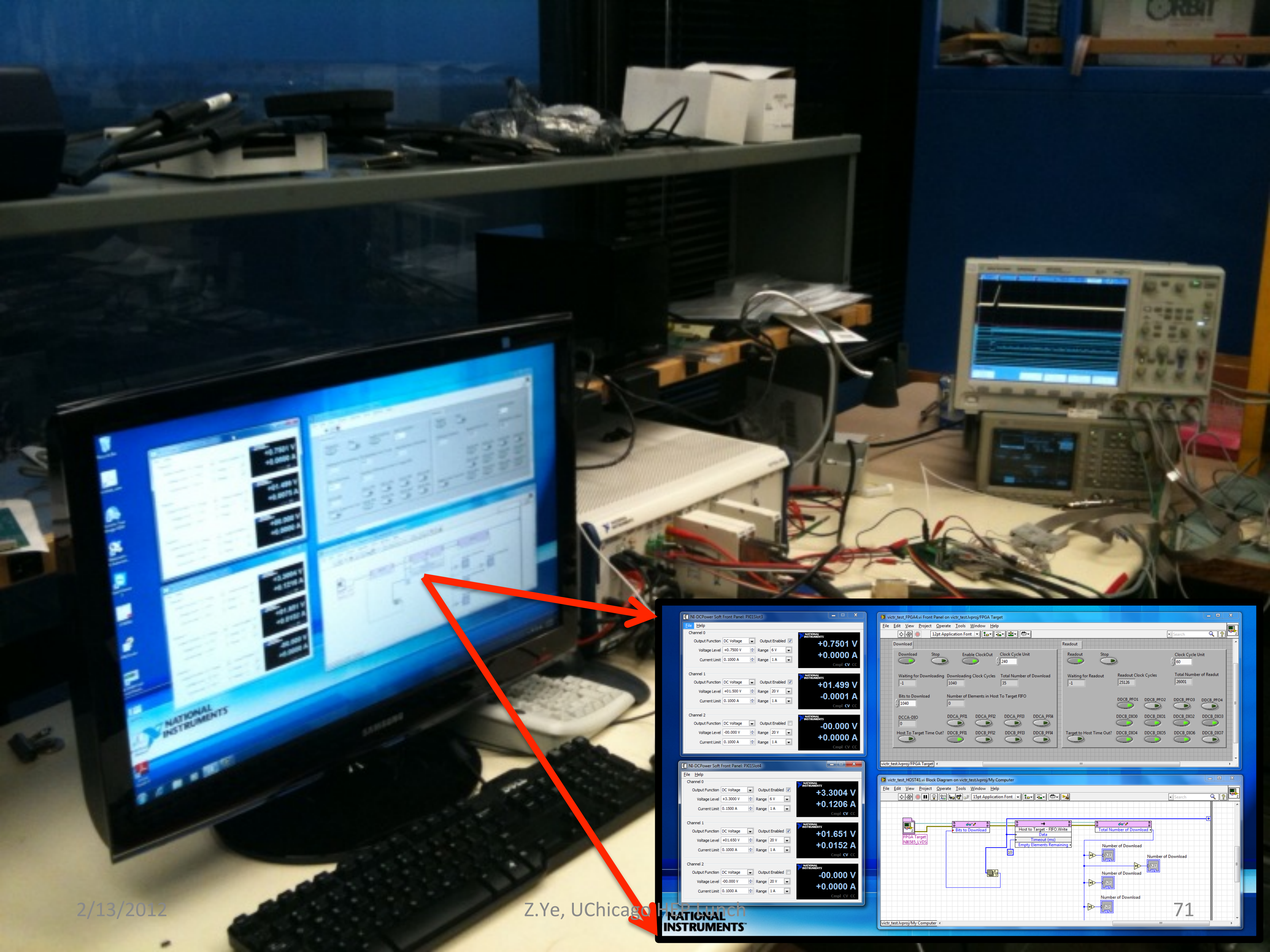




VICTR Test Stand

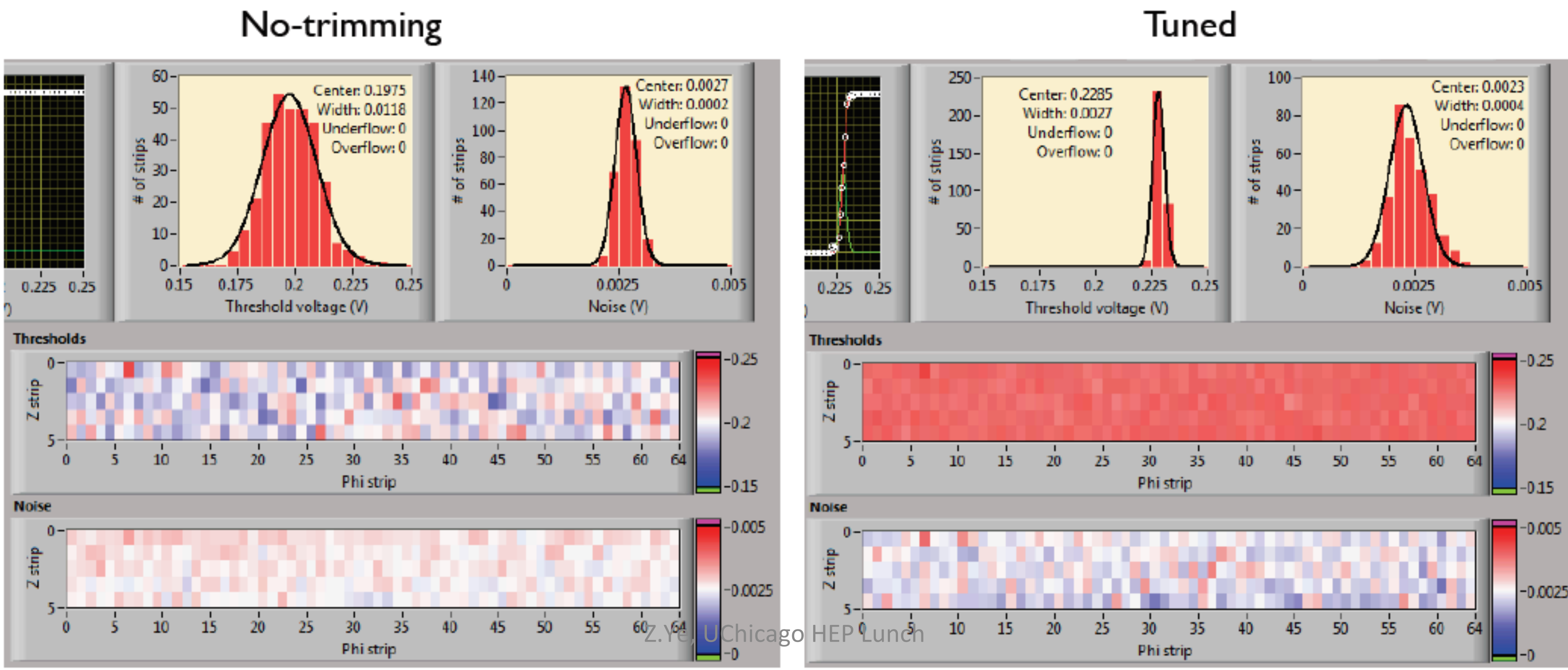
- Two customized PCB boards (passive components+LVDS/CMOS drivers).
- Nantional Instruments FlexRIO system (PC, on-board FPGA module, LVDS I/O adapter module) and Labview.




NI-DCPower Soft Front Panel: PXI1Slot3
+0.7501 V
+0.0000 A
+01.499 V
-0.0001 A
-00.000 V
+0.0000 A
NI-DCPower Soft Front Panel: PXI1Slot4
+3.3004 V
+0.1206 A
+01.651 V
+0.0152 A
-00.000 V
+0.0000 A
NATIONAL INSTRUMENTS

2D Short Strip - Threshold Tuning

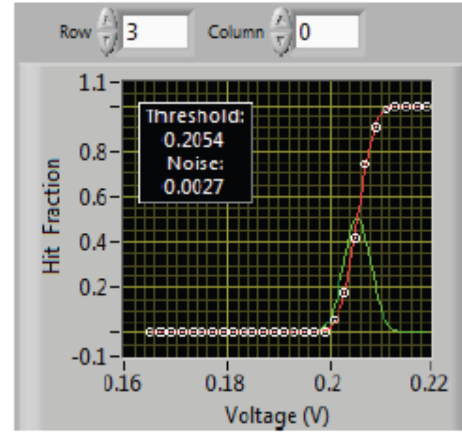
Discriminator threshold for each strip can be controlled independly, allowing for a reduction in the dispersion of the threshold voltages among the strips. Width goes from 12 to 3 mV (to 1 mV after second round)



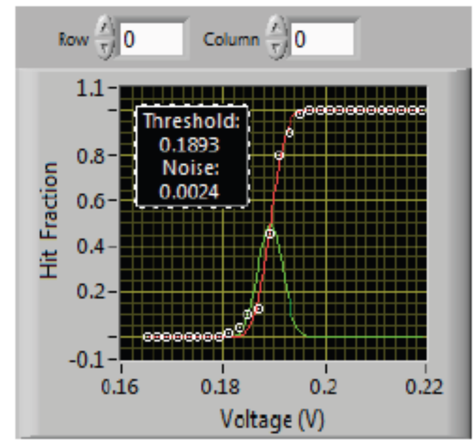
2D Short Strip - Cross Talk

- Found digital to analog crosstalk for specific channels
- We find that within a strip set, if Z<0> has a lower threshold than Z<1-4> and if it is activated at the same time, then the turn-on curve of Z<1-4> becomes like Z<0>'s
- Does not matter if interposing strips are killed or not

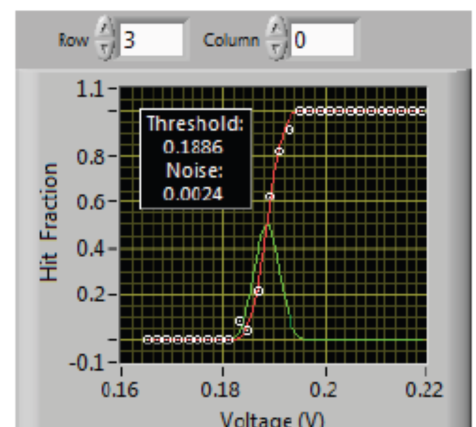
Z3 alone



Z0 alone

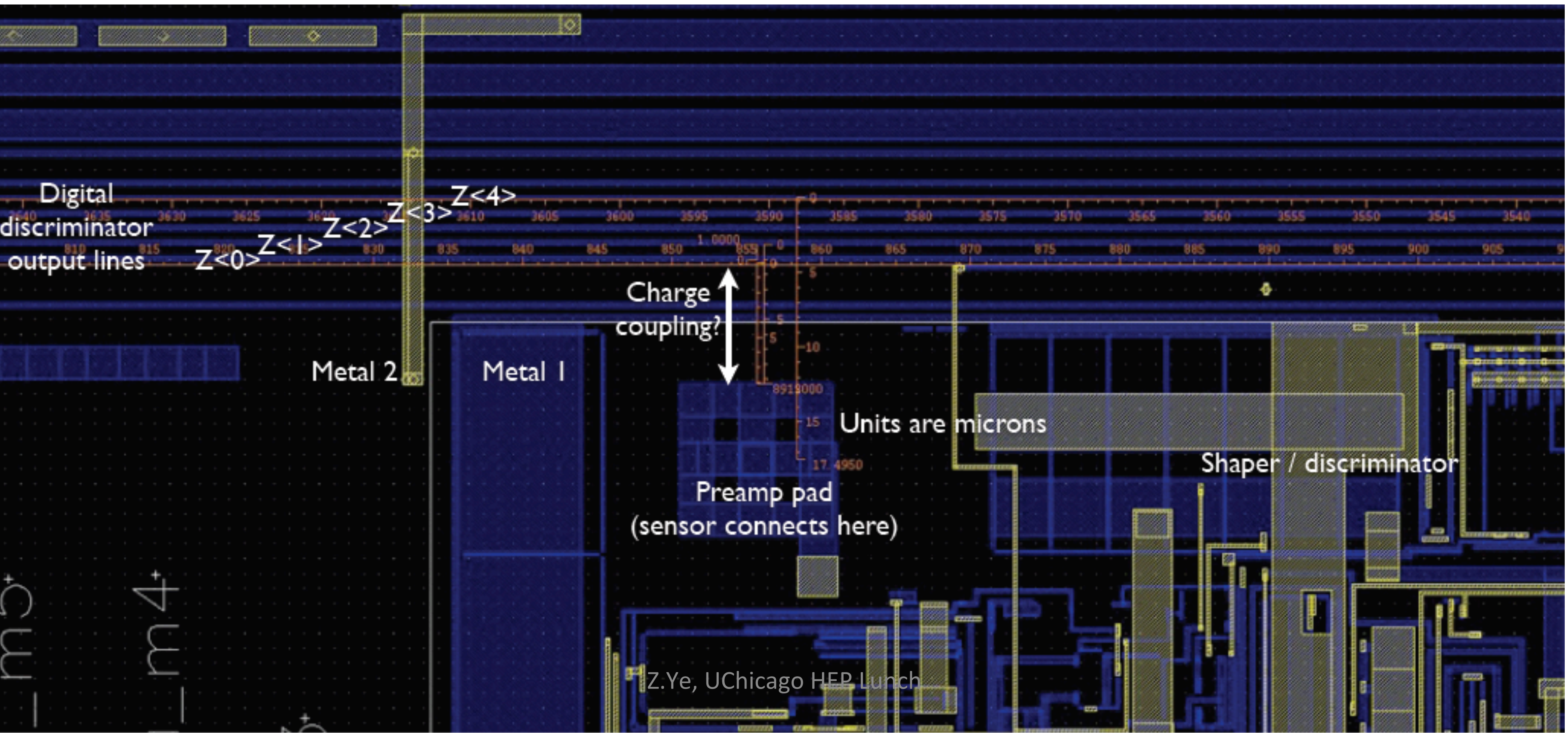


Z3 with Z0 active



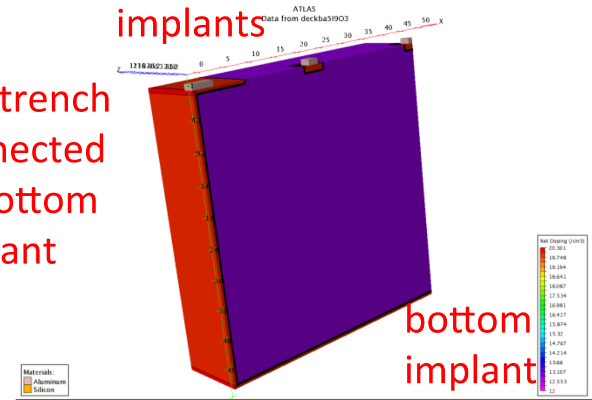
2D Short Strip – Cross Talk

- In each strip set, the 5 discriminator output lines run the same distance to achieve the same capacitance
- This means the Z<0> line runs past each of the sensor pads, 10 microns away
- Induces charge in the subsequent front ends causing lower thresholds

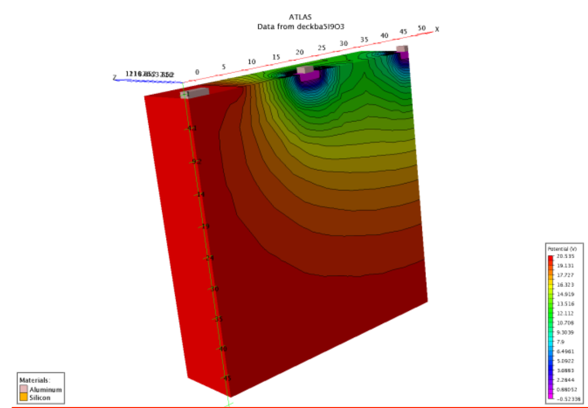


Active Edge Silicon Sensor

- p+ diodes on n bulk (ρ=5kΩ·cm)
- 50 µm deep n++ trench at the edge
  - can use it as a high quality detector edge
  - can use it as an electrode – eliminating edge losses in tiling reticle-sized detectors
- masks designed at Fermilab
- fabricated by MIT-Lincoln Lab



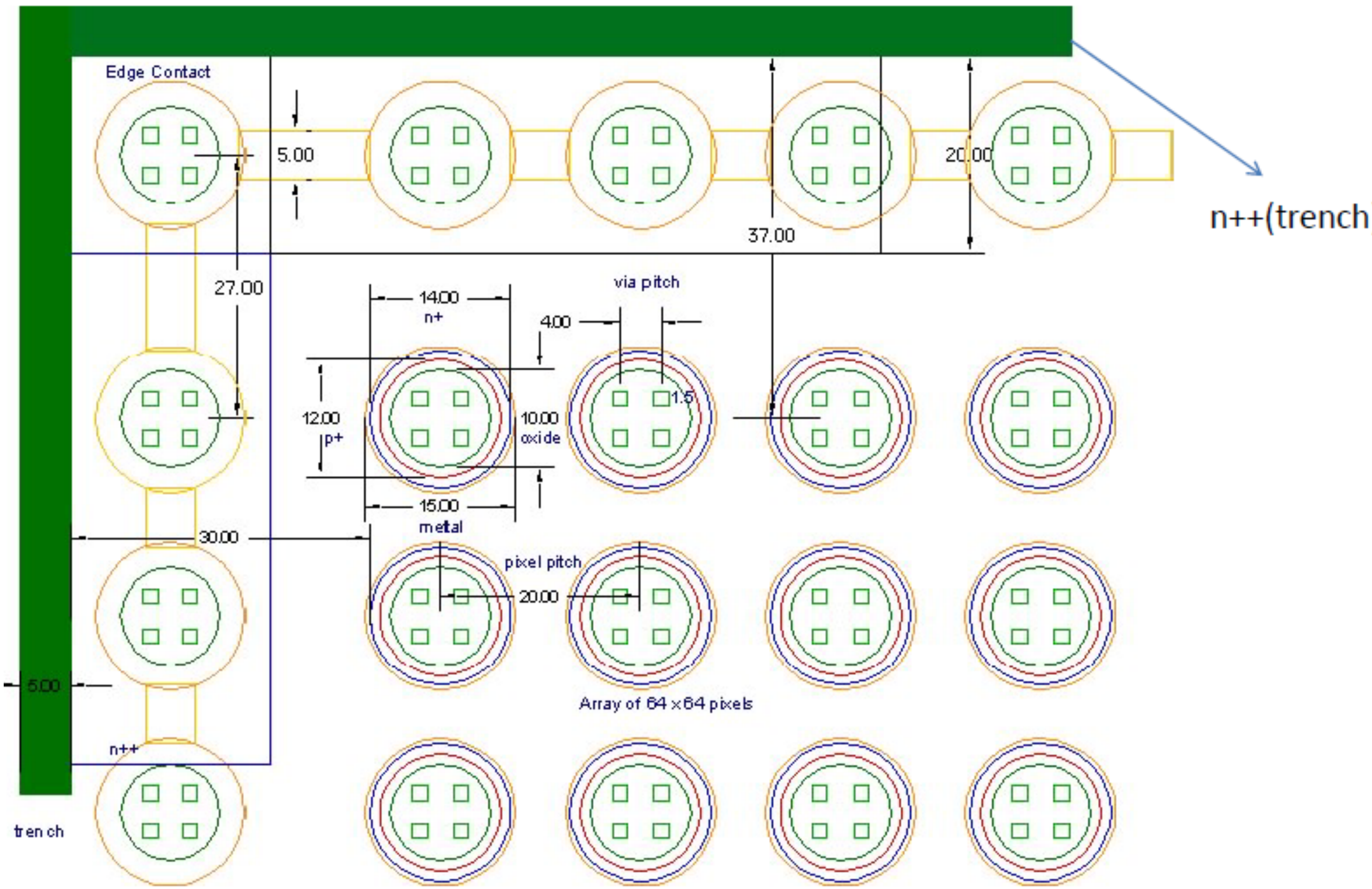
cross section near the edge



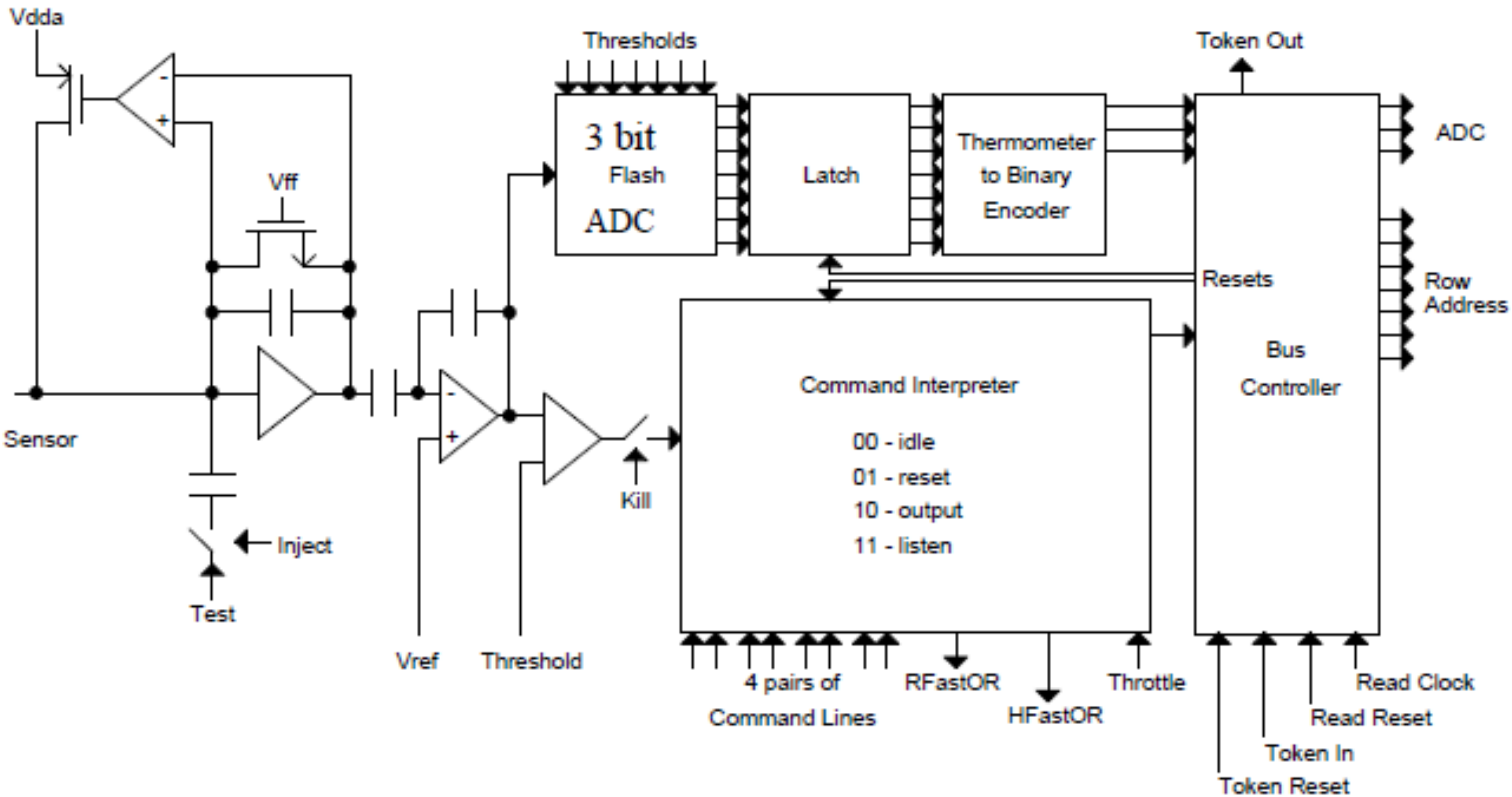
equipotential field lines

Active Edge Silicon Sensor

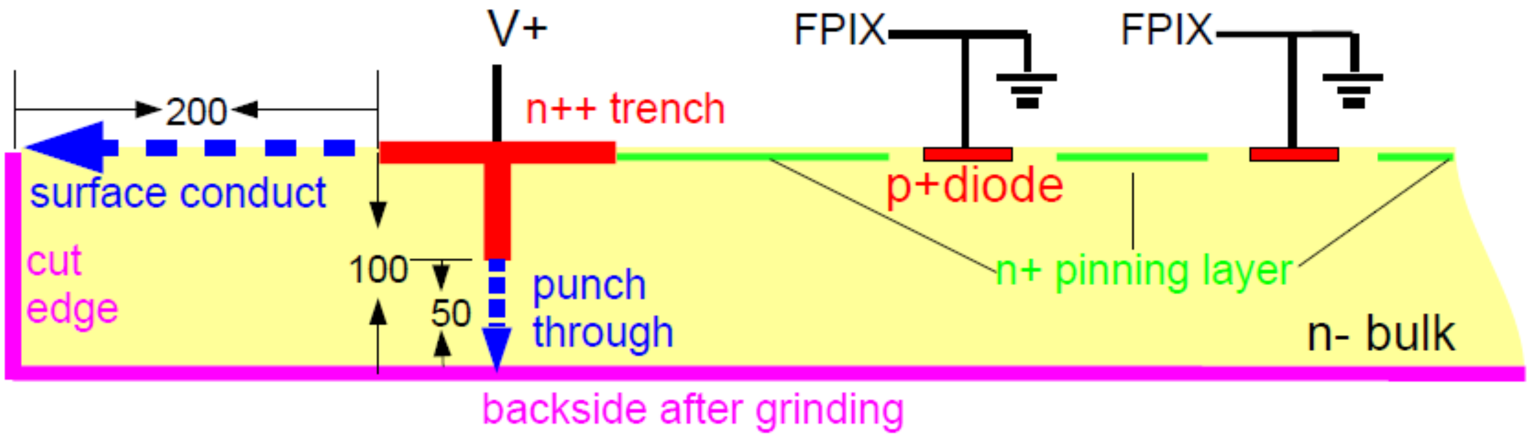
Top view of the pixel array. (20-micron pitch)



BTeV FPIX2.1 Readout Chips

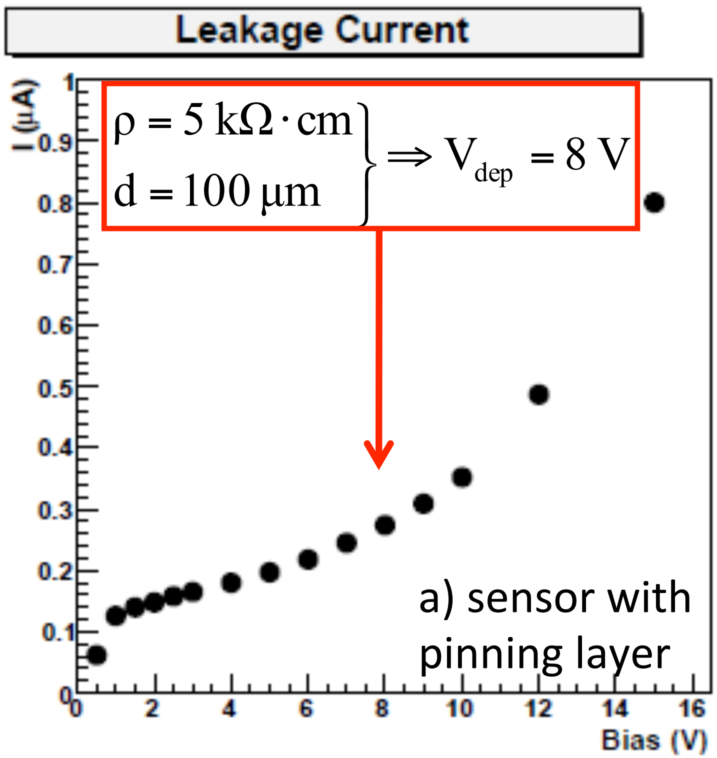


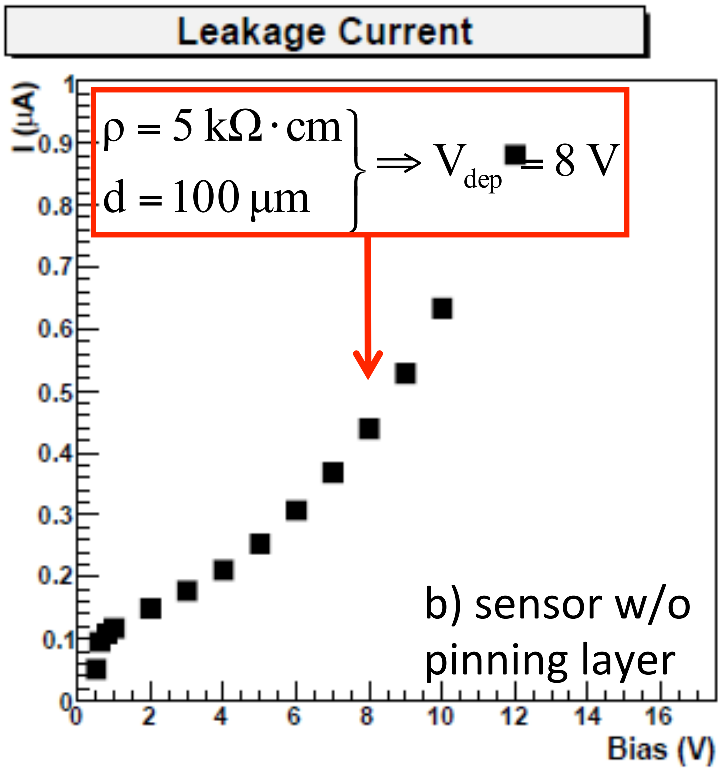
Active Edge Silicon Sensor



- Sensor bias scheme:
  - p+ diodes (DBI) connected to FPIX input at ground potential;
  - n++ trench (DBI) connected to positive potential through FPIX.
- The electrical connection from the trench to the ground surface of the backside might be either (a) along the surface and cut edge or (b) by punch-through 50 μm bulk.
- (optional) n+ pinning layer surrounding p+ diodes and extended to trench:
  - commonly used in optical devices to passivate the detector surface;
  - could act as a shield between the detector and ROIC.

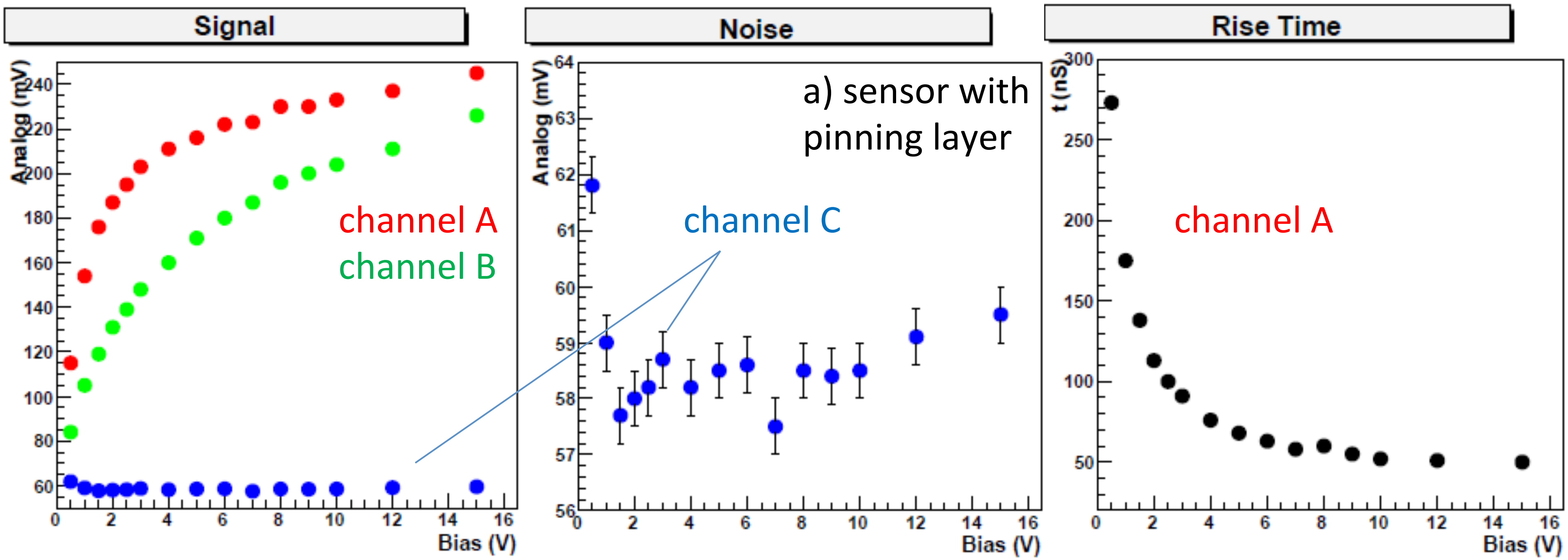
Leakage Current per Chip





- The rapid increase of the leakage current beyond the full depletion voltage is due to the bare ground backside surface and the associated crystal damages.
- Have sent chips to Cornell to further thin the sensors down to 50 μm (include a fine grind process "near-CMP" quality), backside implant and laser annealing.

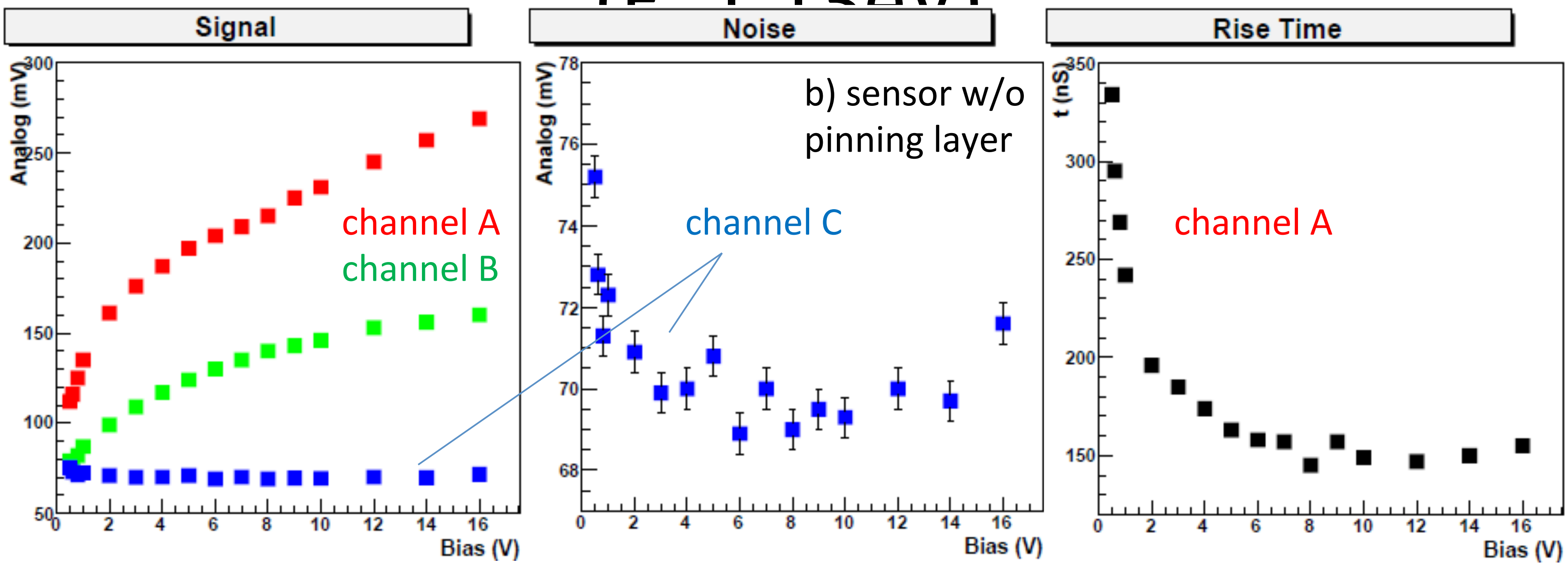
Analog Outputs Due to Laser (E=1.13eV)



Inject a laser onto the sensor backside. Measure the analog outputs of two FPIX channels (A, B) close to the laser, and that of a channel (C) far way from the laser.

- ❑ Amplitude of Anal_Out of A and B increase versus bias – depletion volume increase.
- ❑ Amplitude of Anal_Out of C (interpreted as noise) decreases versus bias – input capacitance of the sensor to the FPIX pre-amplifiler decreases versus bias.
- ❑ Rise time of A decreases versus bias – drifting starts to dominate over diffusion.

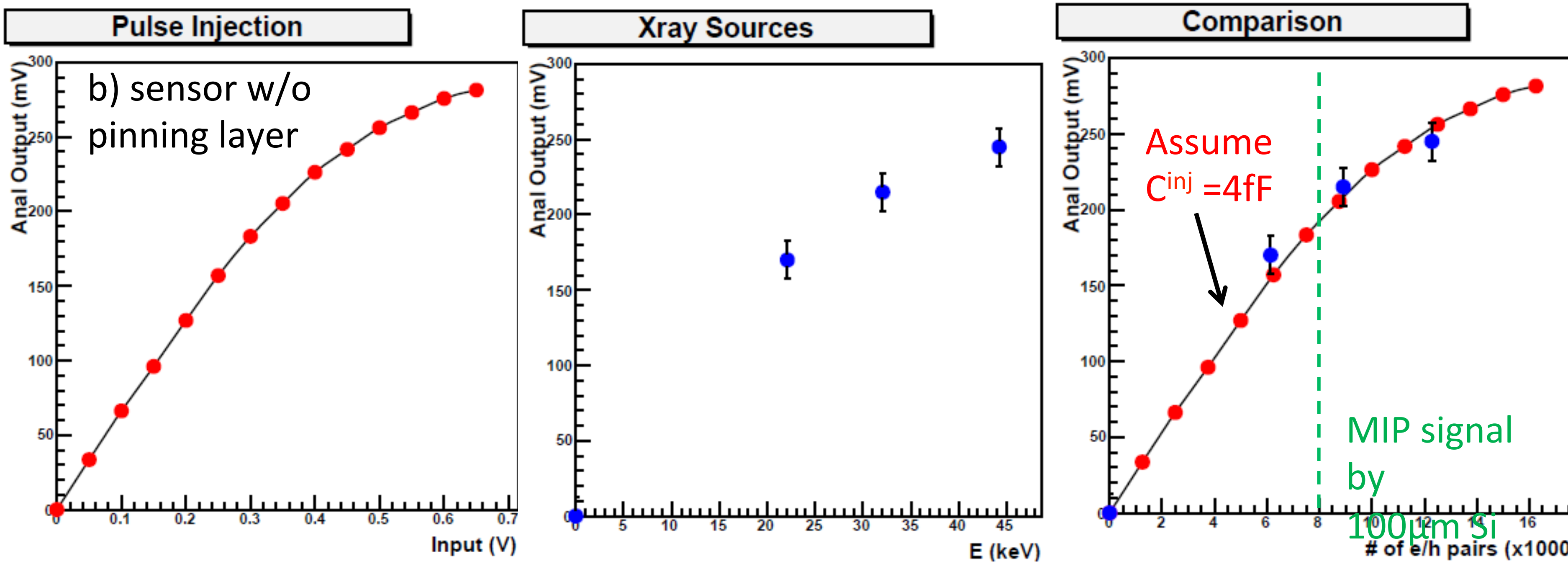
Analog Outputs Due to Laser (E=1.13eV)



Spot a laser on the sensor backside. Measure the analog outputs of two FPIX channels (A, B) close to the laser, and that of a channel (C) far way from the laser.

- ❑ Amplitude of Anal_Out of A and B increase versus bias – depletion volume increase
- ❑ Amplitude of Anal_Out of C (interpreted as noise) decreases versus bias – input capacitance of the sensor to the FPIX pre-amplifiler decreases versus bias
- ❑ Rise time of A and B decrease versus bias – drifting starts to dominate over diffusion

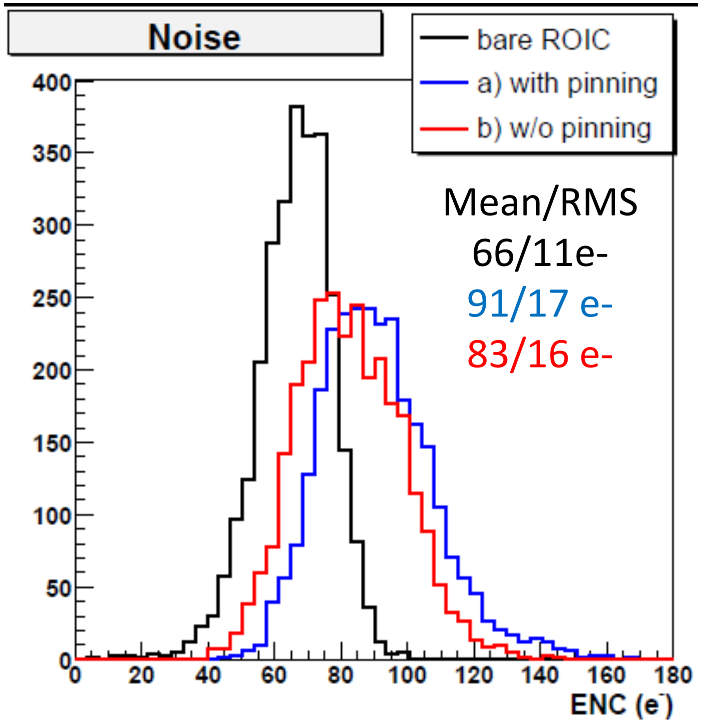
Absolute Calibration Using X-ray Sources

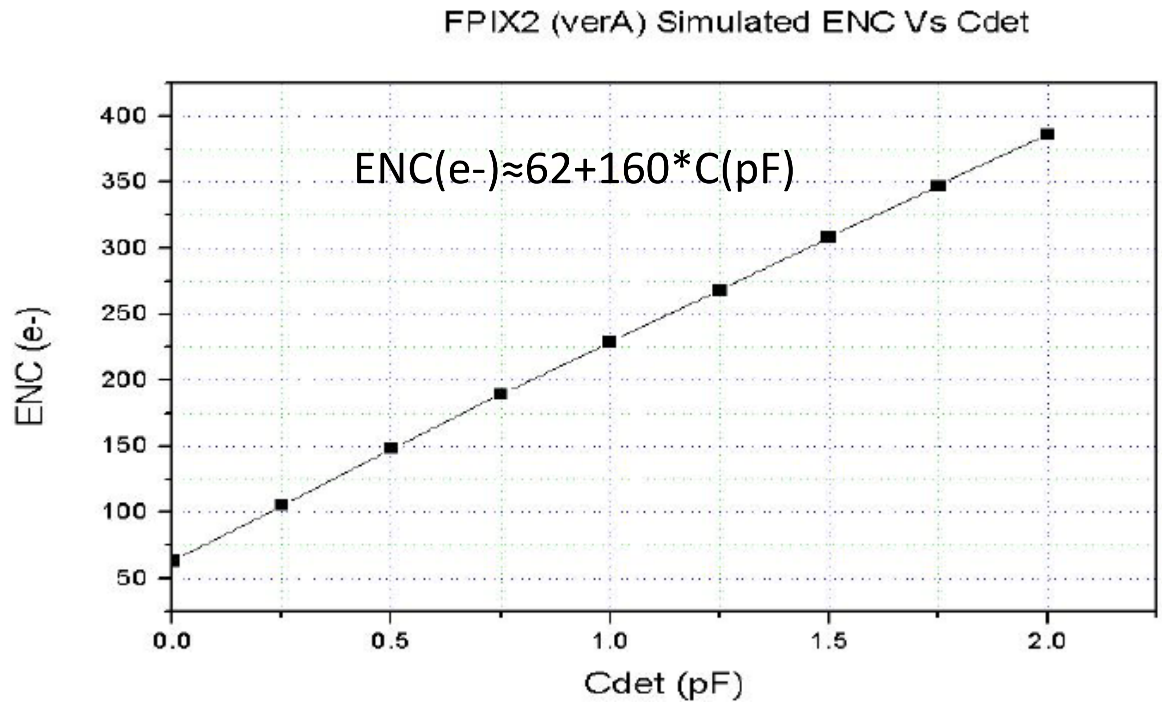


Use a variable X-ray source (metal films in front of Am-241) for absolute calibration:

- ❑measure the (analog output) response curve by charge injection;
- ❑measure (analog output) response to X-ray with different energies (22/32/44 keV);
- ❑converting both of them to # of e/h pairs (to constrain injection capacitance C^{inj}).

Sensor Input Capacitance to FPIX2.1



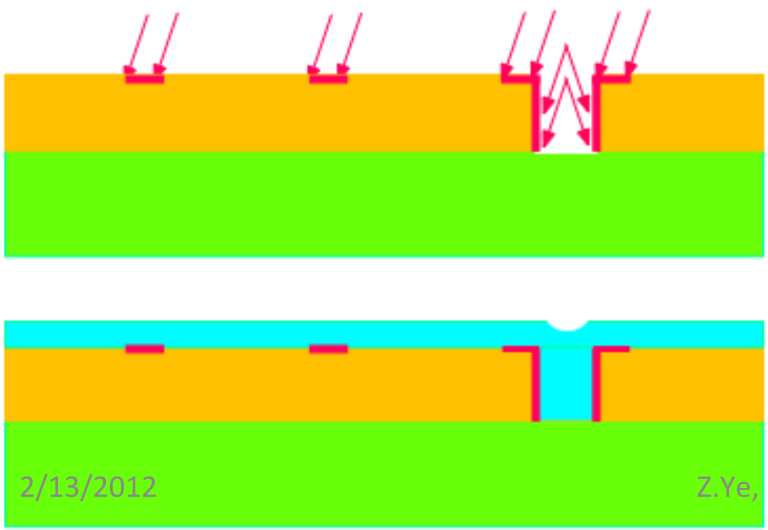


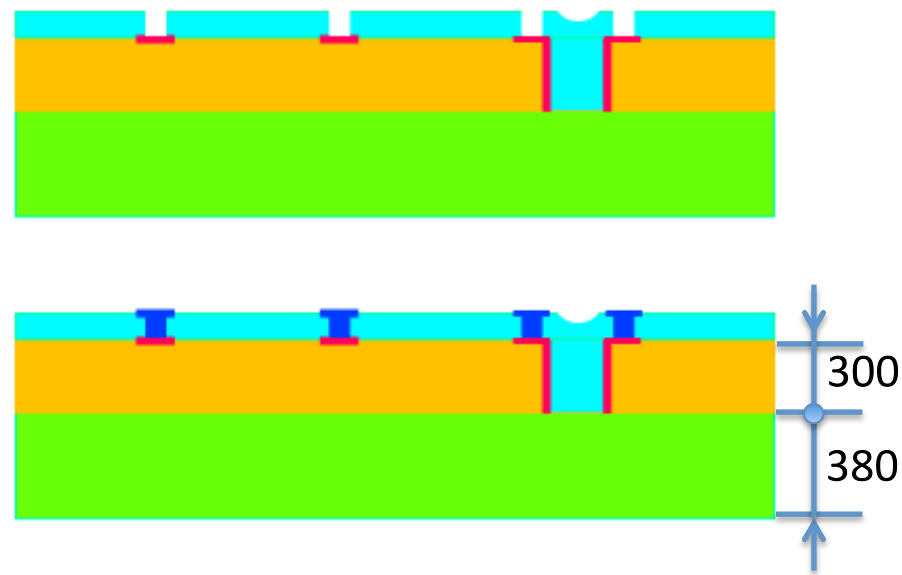
Conversion from the test pulse size to the number of electrons done assuming 3.5fF injection capacitors. Absolute calibration underway.

a) with pinning layer C=0.155 pF

b) w/o pinning layer C=0.106 pF

Active Edge Silicon Sensor





Trench filled with oxide or polysilicon?
(MIT-LL wafers had poly fill)