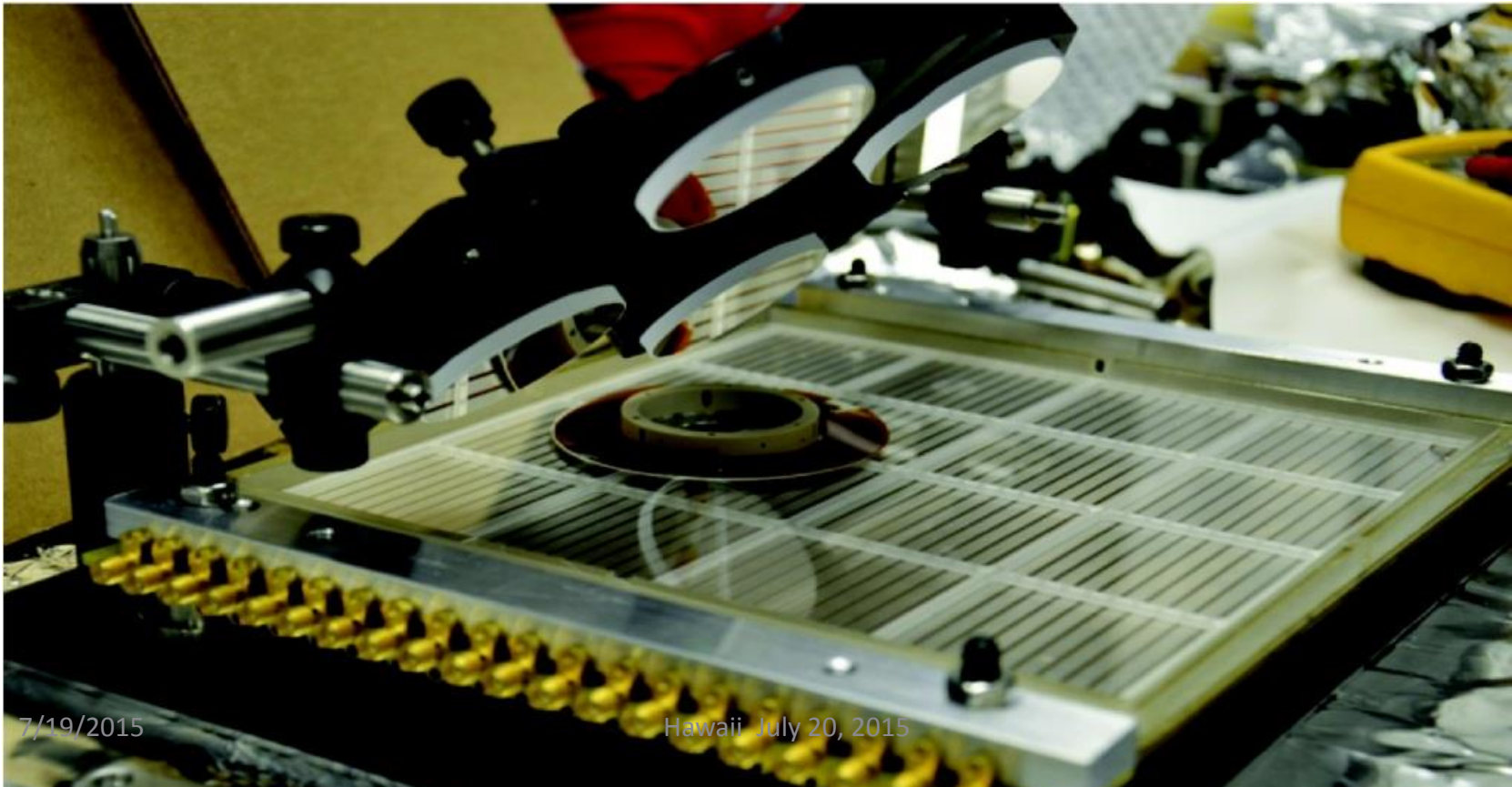


The University of Chicago PSEC Group Goals, Status, and Requests

Andrey Elagin, Henry Frisch, Carla Grosso-Pilcher, Mary Heintz, Rich Northrop, Eric Oberla, Matt Wetstein; Brooke Adams, SiYang Ling , Eric Spieglan (undergrads)
Enrico Fermi Institute and Physics Department
University of Chicago



The Large-Area MCP-PMT

A Transformational Technology

- No competition in time resolution, gain-bandwidth, number of pixels per area, noise
- No competition in scalability to large areas
- Intrinsically simple and components are cheap
- Millions (almost a billion) of pixels per m^2 each with psec time resolution opens up opportunities that have never been considered.

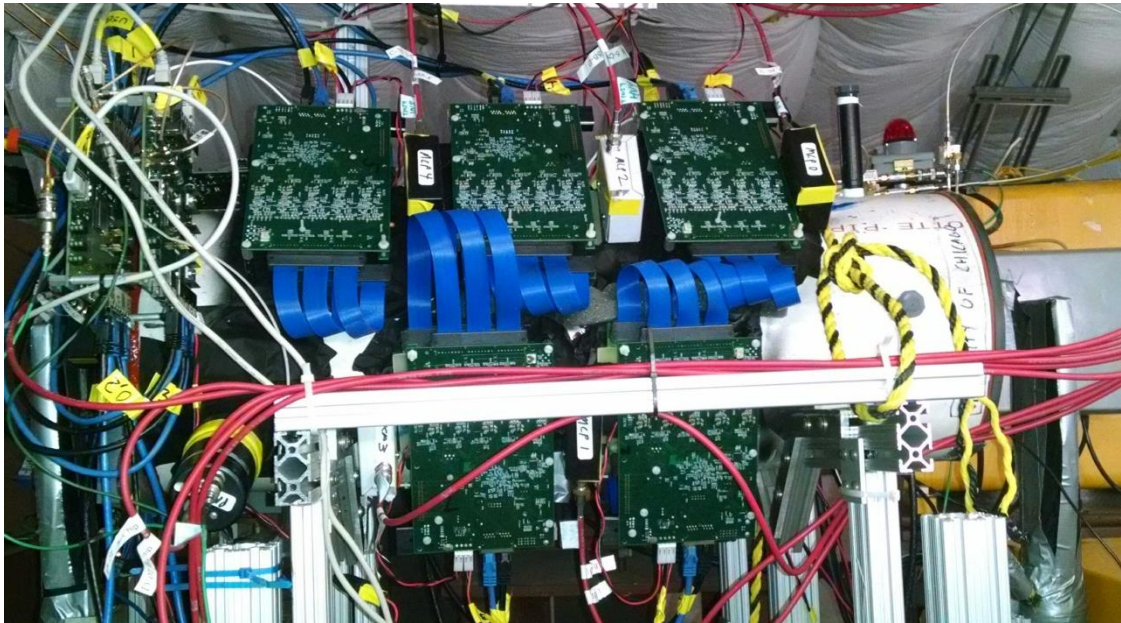
WE HAVE FOUND NO SHOW-STOPPERS AND THERE IS NO COMPETITION IN PERFORMANCE

However it is not easy...we have both successes & challenges

Part I. The Optical Time Projection Chamber

(great name – thanks to Howard Nicholson, who also suggested applying LAPPDs to neutrino detectors)

Ph.D Thesis of Eric Oberla- July 31. (to be a NIM paper)



The OTPC installed in the LArIAT beamline in Mcenter at Fermilab

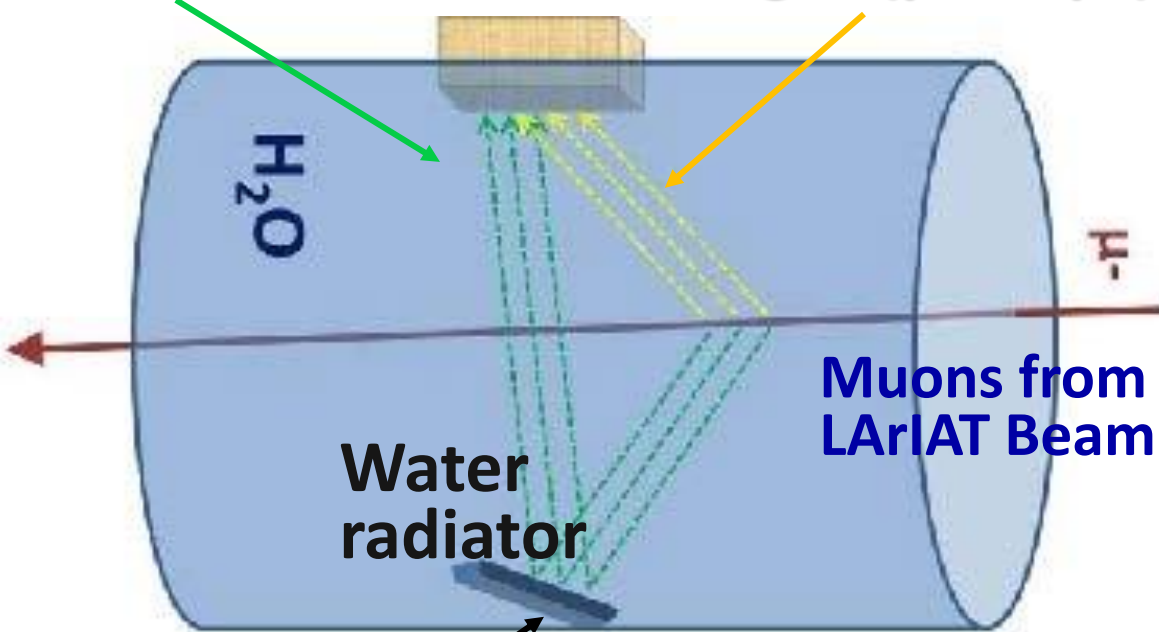
Demonstration device for a new kind of detector-reconstructing tracks using precise measurements of light transit times and arrival locations. Related to possible uses in HEP, nuclear, and security – intended to demonstrate that one can reconstruct tracks in a simple small water volume.

The First Optical Time Projection Chamber

Ph.D Thesis of Eric Oberla- July 31. NIM paper

11"

Reflected Cherenkov Light (1000 psec later) Direct Cherenkov Light (prompt)



Mirror for each Planacon (5)



30"

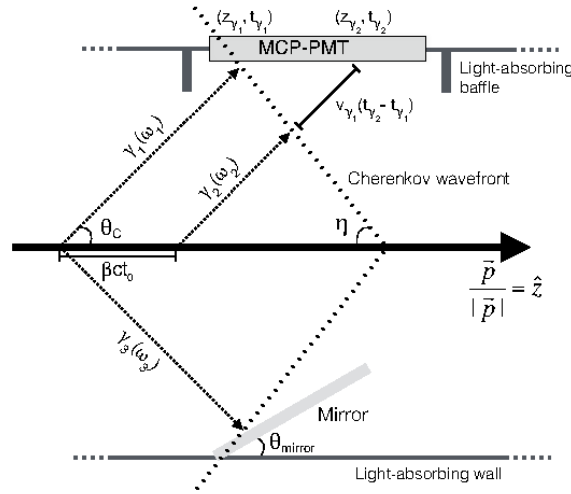
Ports for Planacon MCP-PMTs (3 normal, 2 stereo) equal spacing in z

Ack: Home Depot

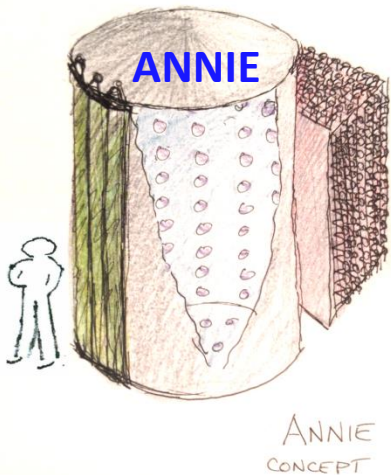
The OTPC exploits 3 ideas possible only with fast (“psec”) photodetectors

- 1. ‘Drift’ photons by measuring the arrival times. Measures the distance to photon origin (3D point vs the 2D arrival position)**
- 2. Multiply effective photocathode area x QE by using mirrors. The prototype design conservatively gains a factor of 2. Exploits the ‘room’ in the time dimension.**
- 3. Use 50-Ohm transmission-line readout with only half the number of electronics channels by using the ‘bounce’ of unterminated delay lines on the anode (EO)**

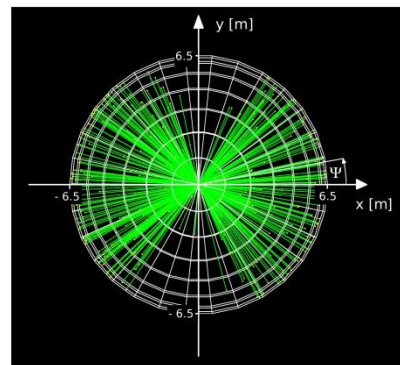
'Drifting' Photons- exploit Cherenkov rad.



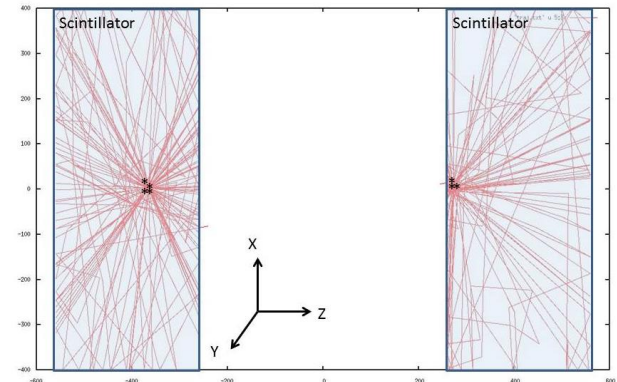
The principle of reconstructing the track position and direction is the same in **HEP neutrino physics (ANNIE)**, **nuclear neutrino-less double-beta decay (JINST paper)**, and **TOF-PET imaging (prov. patent)**.



Double-beta decay



TOF-PET



Longitudinal vs Transverse Phase Space

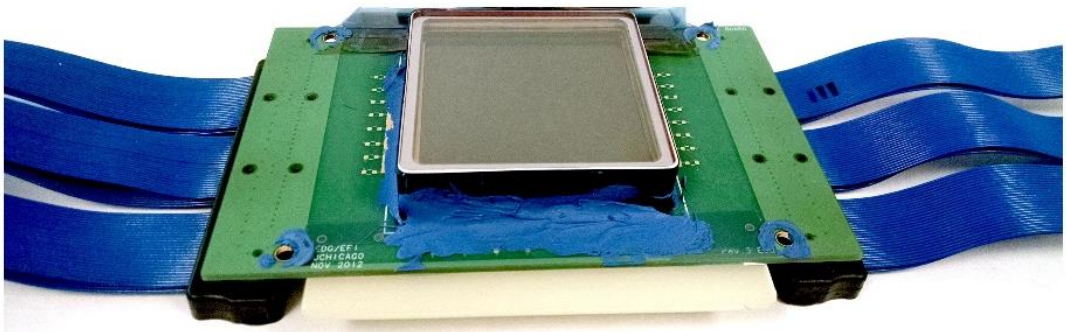
Each photodetector, in both normal and stereo views, in the OTPC prototype has a corresponding flat mirror that reflects the light going diametrically opposite back onto the detector. Photons can arrive at the same point but are distinguishable by the difference in arrival times. This extra 'room' in phase space:

- **Economically doubles the effective photocathode area (mirrors are much cheaper than tubes);**
- **Measures points on the track via the difference in the arrival times of direct and reflected photons (one gets earlier and the other later for transverse displacements)**
- **May allow some clever designs for large detectors by exploiting the presence of both longitudinal (time) and transverse (position at the photocathodes) phase space to increase coverage more than just twice, and to cover less simple geometries (emittance manipulations like those in accelerators).**

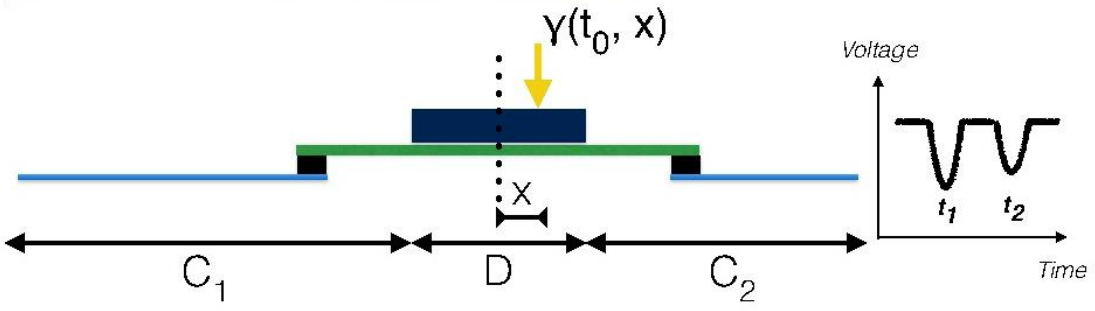
Exploiting the GHz Transmission Line Anode

Eric Oberla

1 end of 50 Ohm TL is unterminated stub



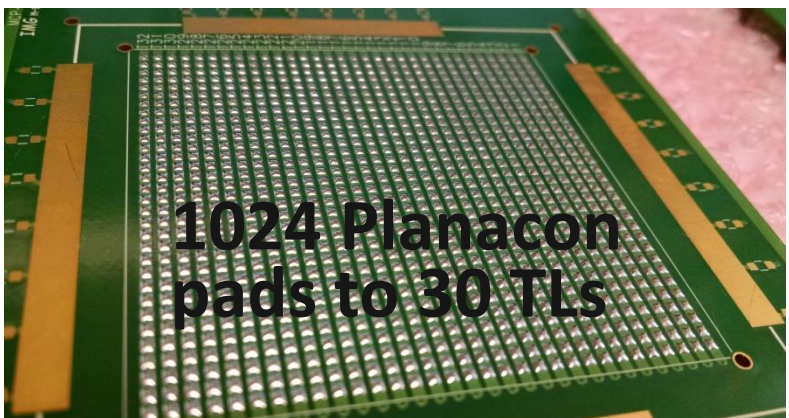
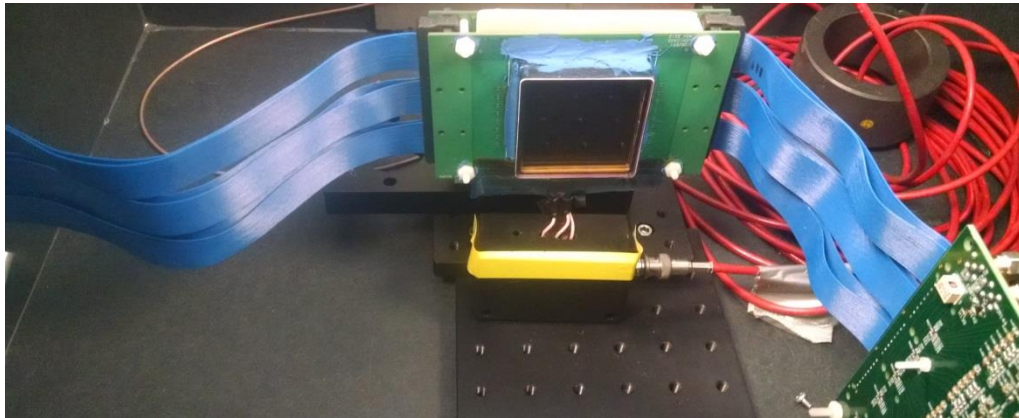
This end read out by PSEC4 ASICs



which see the pulses from both ends of the TL on the same channel - do the autocorrelation read out by PSEC4 ASICs

unterminated stub

PSEC4 ASICS

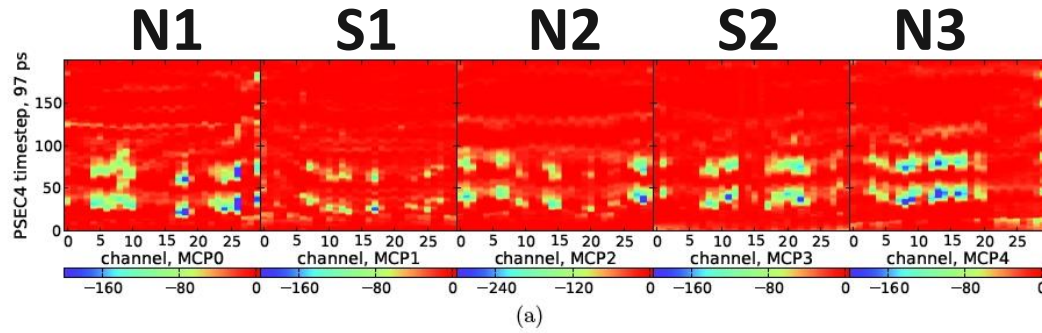


1024 Planacon pads to 30 TLs

We see tracks in the water. 'Typical Events'

Front-back
Trigger

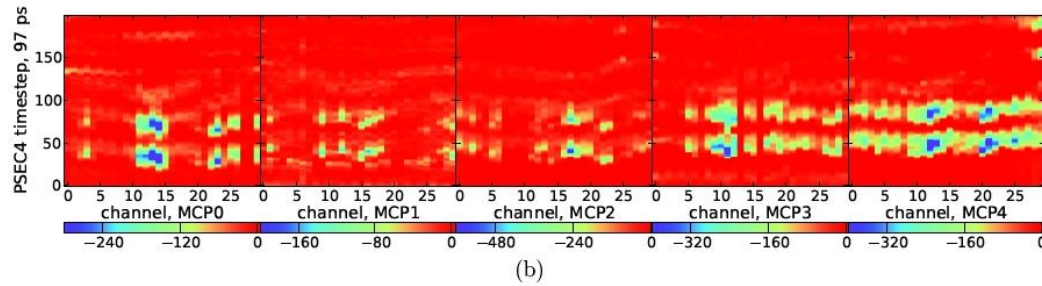
Time



Through

Front-back
Trigger

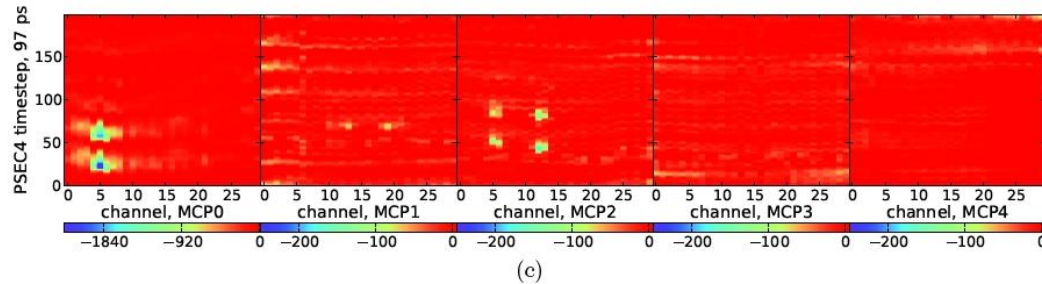
Time



Showering?

Front-only
Trigger

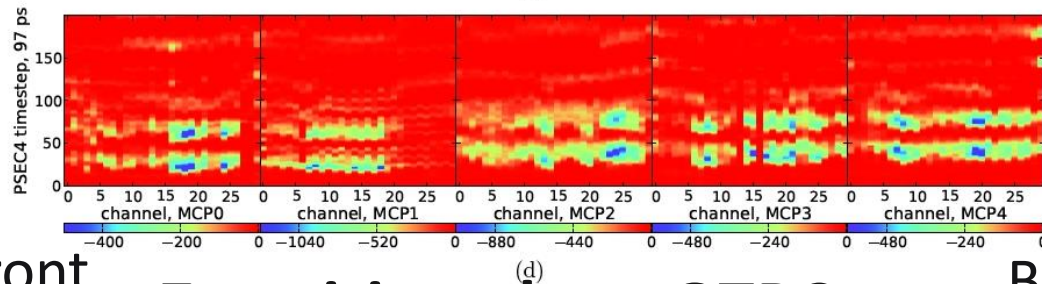
Time



Big splat (?)

Front-only
Trigger

Time



Through

Front

Z position along OTPC

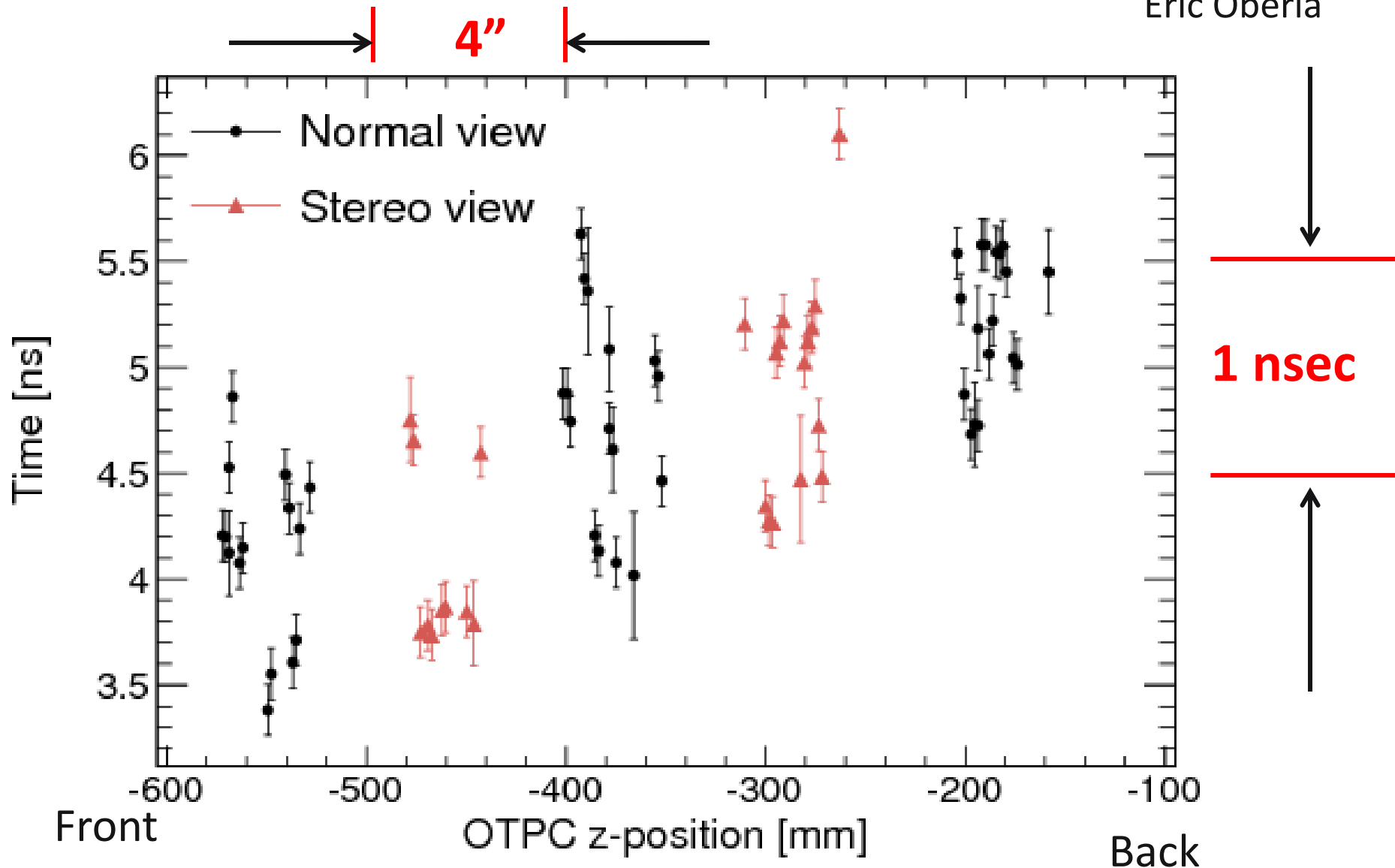
Back

Note: this is pedestal-subtracted raw data . Scale is 0 to -3000 counts

Eric Oberla 9

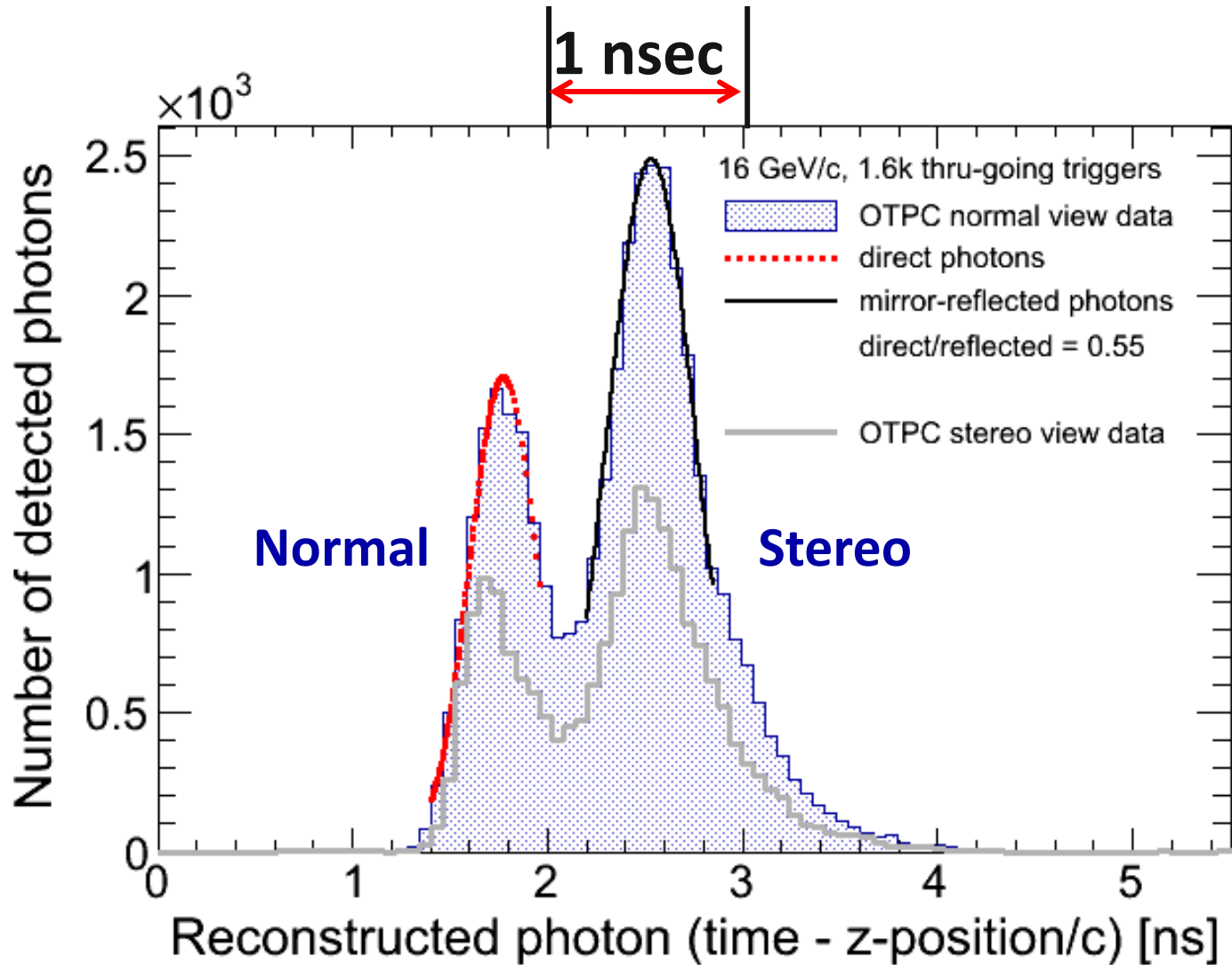
Preliminary Analysis – Tracks

Eric Oberla



Resolving the Direct and Reflected Photons

Eric Oberla

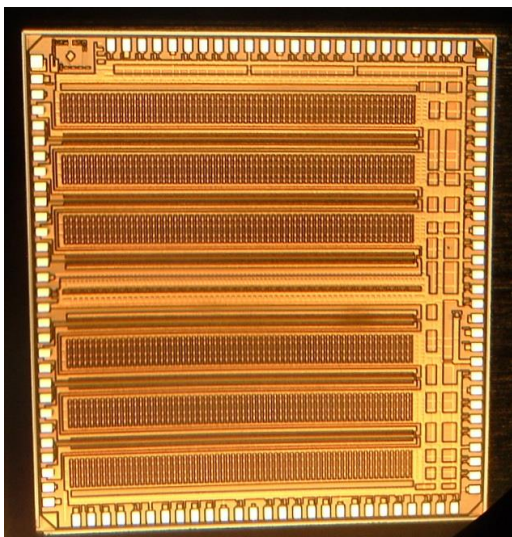


Preliminary Conclusions

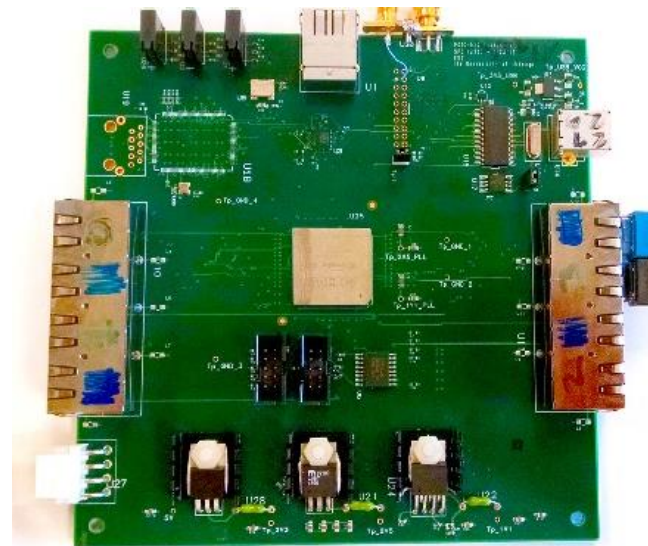
- These data were taken May 19- Eric has written the analysis programs between then and now, so all is preliminary
- The hit-finding efficiency is $\geq 75\%$ of predicted- a victory. The loss is consistent with the deficiency seen in the direct view, consistent with light cut off by the baffle of the MCP-PMT housing (i.e. fixable).
- It looks nice. The Demountable LAPPDTM data have $\sim 10X$ the gain of these Planacons, and should work at least as well over $16X$ the area/photodetector.
- Eric has done a remarkable job- he built the detector basically single-handedly. Detector development makes for good students!* Ph.D thesis and NIM paper next.

* (Steinberger's question at CERN-
Why do Americans build such lousy detectors and have such good students?)

Part II. UC Electronics and Readout Systems



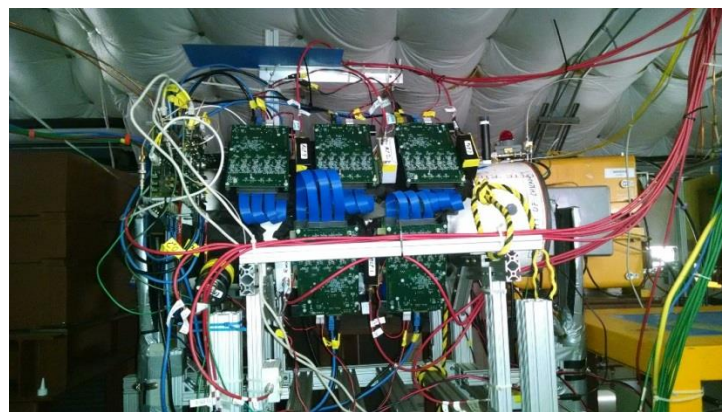
PSEC-4 ASIC



Central Card (4-ACDC;120ch)



30-Channel ACDC Card (5 PSEC-4)



180-channel OTPC system

PSEC4 evaluation board

- 6-channel, 1.5 GHz, 10-15 GSa/s evaluation module
- USB 2.0 / powered over USB
- For best results, put in an RF box

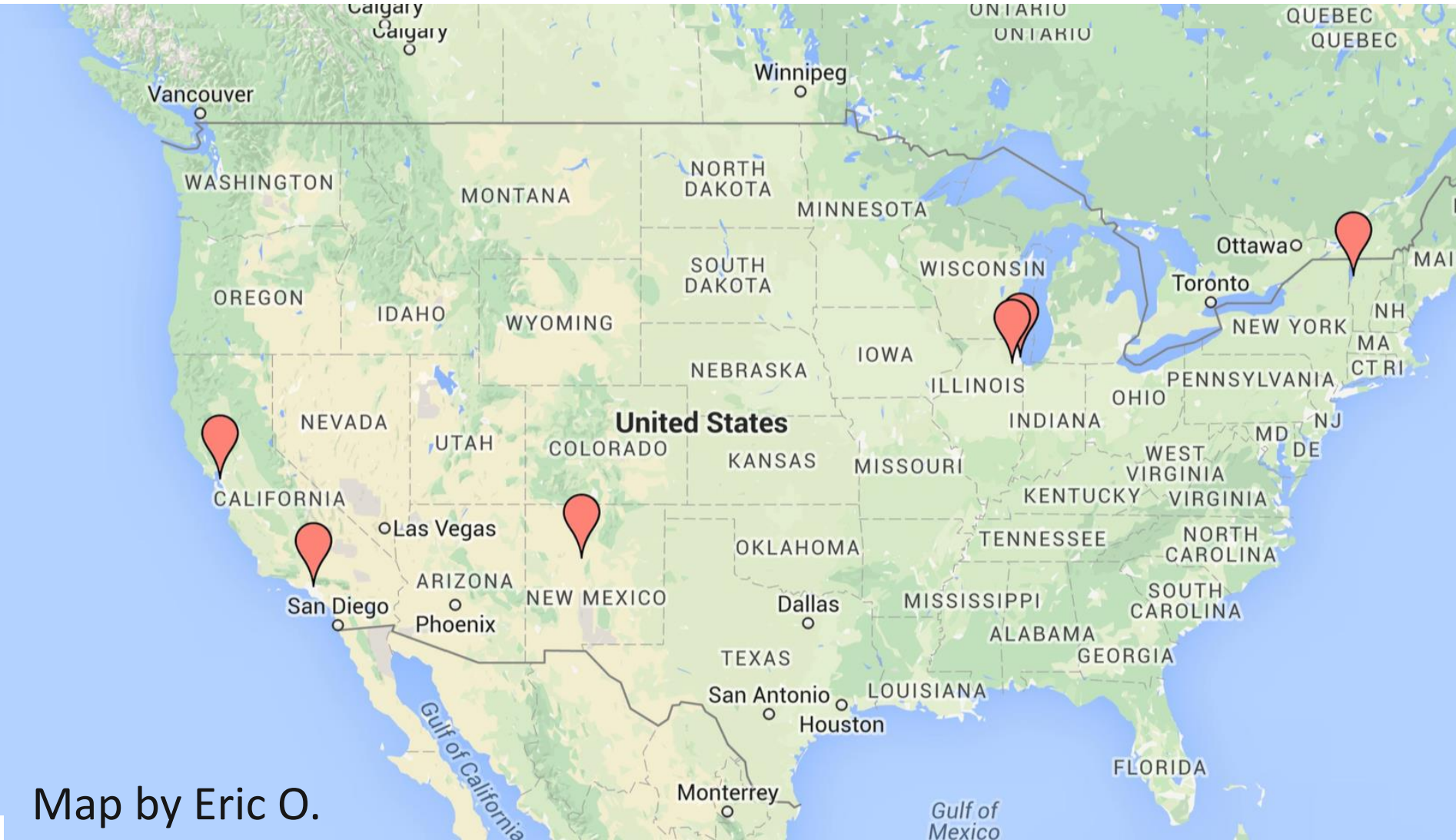


Motherboard designed by M. Bodgan (EFI/eshop)

Eric slide (mostly)

PSEC4 evaluation board

Recent additions: Iowa State, LLNL, ... (5 new bds by Sandia)



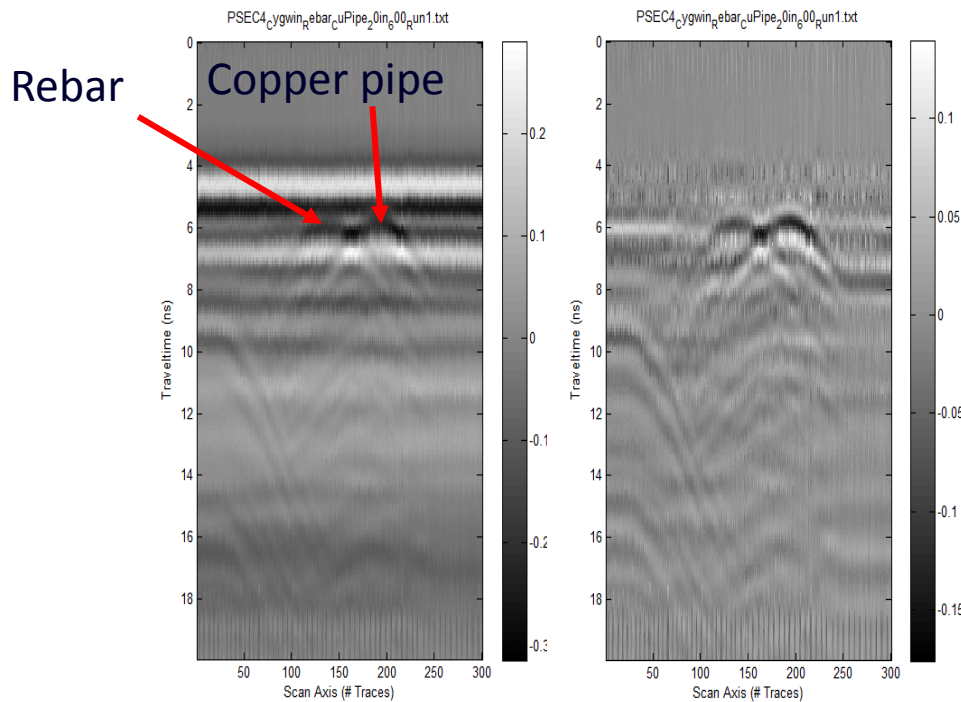
Map by Eric O.

Example of PSEC4 Adoption for Road and Bridge Infrastructure: D. Huston's GPR group at Vermont

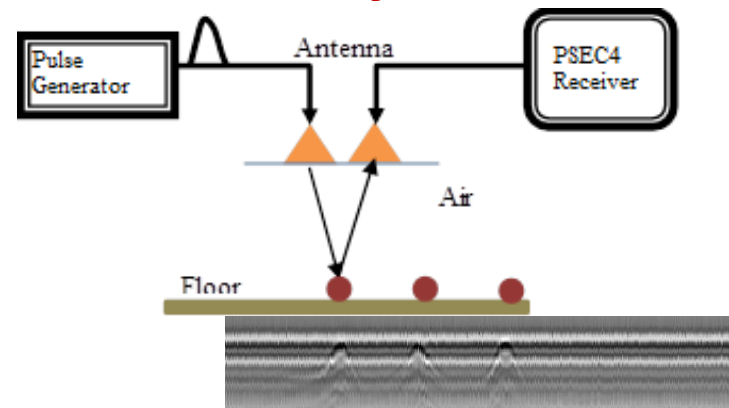
Ground penetrating radar:
Development of a High Speed UWB GPR for Rebar Detection

Advantages in cost, size, power, scalability

- Operate at road speeds (60 mph)
- Capture and process real-time data
- Multi-channel
 - Physical coverage across width of roadway
- Meet or exceed FCC mask requirements
 - FCC 02-48 compliant
- Compact, modular design

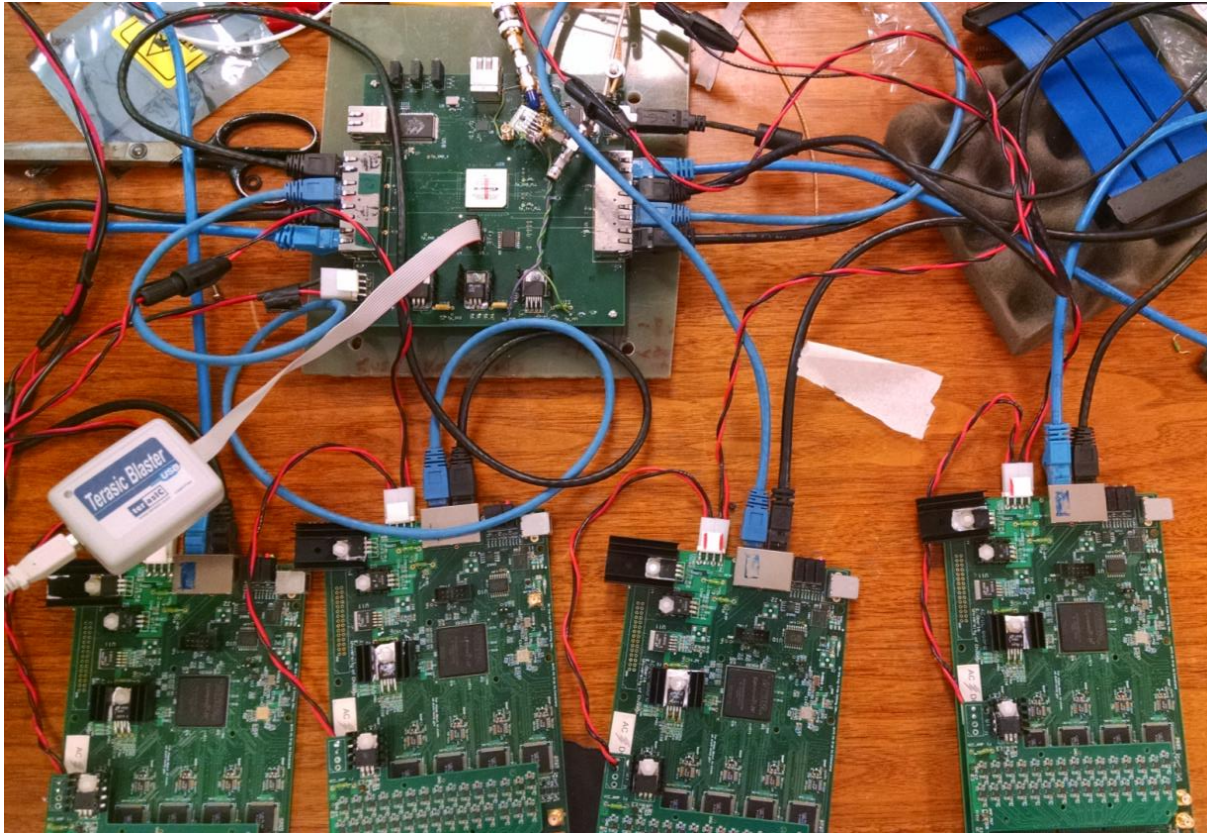


E. Oberla slide (mostly)



Tests using metal bar as a reflection target using the WFS-ASIC system. The goal is to be able to measure reflections from subsurface objects, such as steel reinforcing in concrete and buried utilities.

Multichannel systems



- 60-channel Demountable at the APS Laser Lab (ANL X-ray Science Division)- dismantled
- 180-channel **self-triggered** OTPC at Fermilab
- Current Central Card supports 240 channels
- Central Cards can be `daisy-chained` for 480 ...

Working on Gen-II Central Card

Design by Mircea Bogdan on Watchman funds: reuses blocks from Wah's JPARC and other working boards by Mircea

- **Higher-speed and more options for readout:- USB, Ethernet, & 6Gbps/fiber QSFP+;**
- **Can handle 8 ACDC cards for a total of 240 channels per module (twice 1st Gen)- multiple modules can be daisy-chained;**
- **Expanded system, trigger, signal interfaces for flexibility in use:**
 - **one RJ45 connector with LVDS for system integration;**
 - **8 RJ45 connectors with LVDS for Front End Cards (FE)communication.**
 - **SMA inputs to FPGA I/O on front-panel for trigger or optional clock input**
 - **several other SMA inputs on board for app-specific signals**
 - **inputs/outputs from FPGA**
- **Implemented in a widely-used standard: VME32/64X**

Gen-II Central Card (Mircea Bogdan)



A 500 MHz sampling VME board by Mircea for KOTO - many of the blocks/components will be re-used in the Gen-II Central Card

New PSEC-4 MOSIS Run

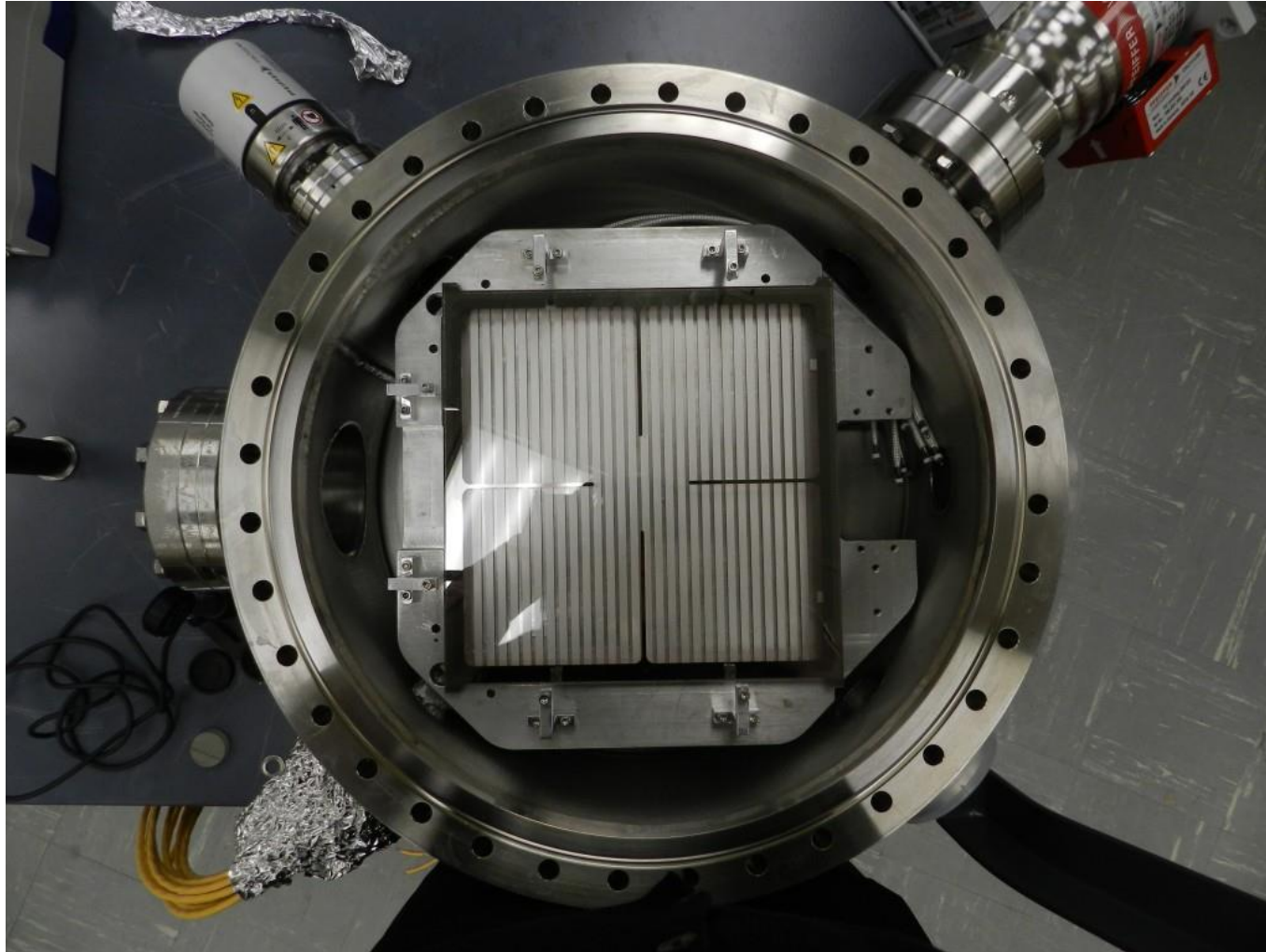
- Although PSEC-4 has short-comings, it works well, is well-documented (long NIM paper), and can sample up to 15 GS/sec with a bandwidth of 1.6 GHz;
- ASICs are not easy- decided to double-down on the investment in PSEC-4's speed and bandwidth;
- Sandia (NM) paid the NRE and bought a 2nd run from MOSIS- we piggy-backed and bought 2 lots of 40 chips for 10K\$ each (standard price);
- MOSIS offered us a deal of 3K\$/batch (reduced from 10K) after the NRE if we bought 135K\$ total; Iowa, MIT, Sandia-NM, Sandia-CA, and UC have jointly ordered it (1200 chips);
- ANNIE, Nu-DOT, Sandia use in short-term--other trials of psec -(<5) resolution wave-form sampling in progress

Beyond PSEC-4

(See Kurtis's talk on the Hawaii/UC coordinated effort)

- Main limitation of PSEC-4 is the 256-cell buffer- Eric has gotten the self-triggering to work, so that a global trigger can come in after the signals, but it incurs deadtime and isn't applicable to high occupancy or high rate applications
- We and Gary's group have been working on PSEC-5, a joining of the PSEC-4 sampling design with Gary's deep buffer design, but moved from IBM to TSMC. We've done much of the front-end, but had to stop as the 2014 ARL funding for this task was cut.
- Gary and Innosys (SLC) and us have an SBIR for PSEC-5 development- Hawaii playing the leading role;
- Eric has proposed a PSEC-4A that makes minimal changes (sic) to PSEC-4 beyond adding multiple buffering of hits so that it's deadtimeless for typical neutrino experiments (e.g. ANNIE). Attractive to me (in parallel to PSEC-5) .

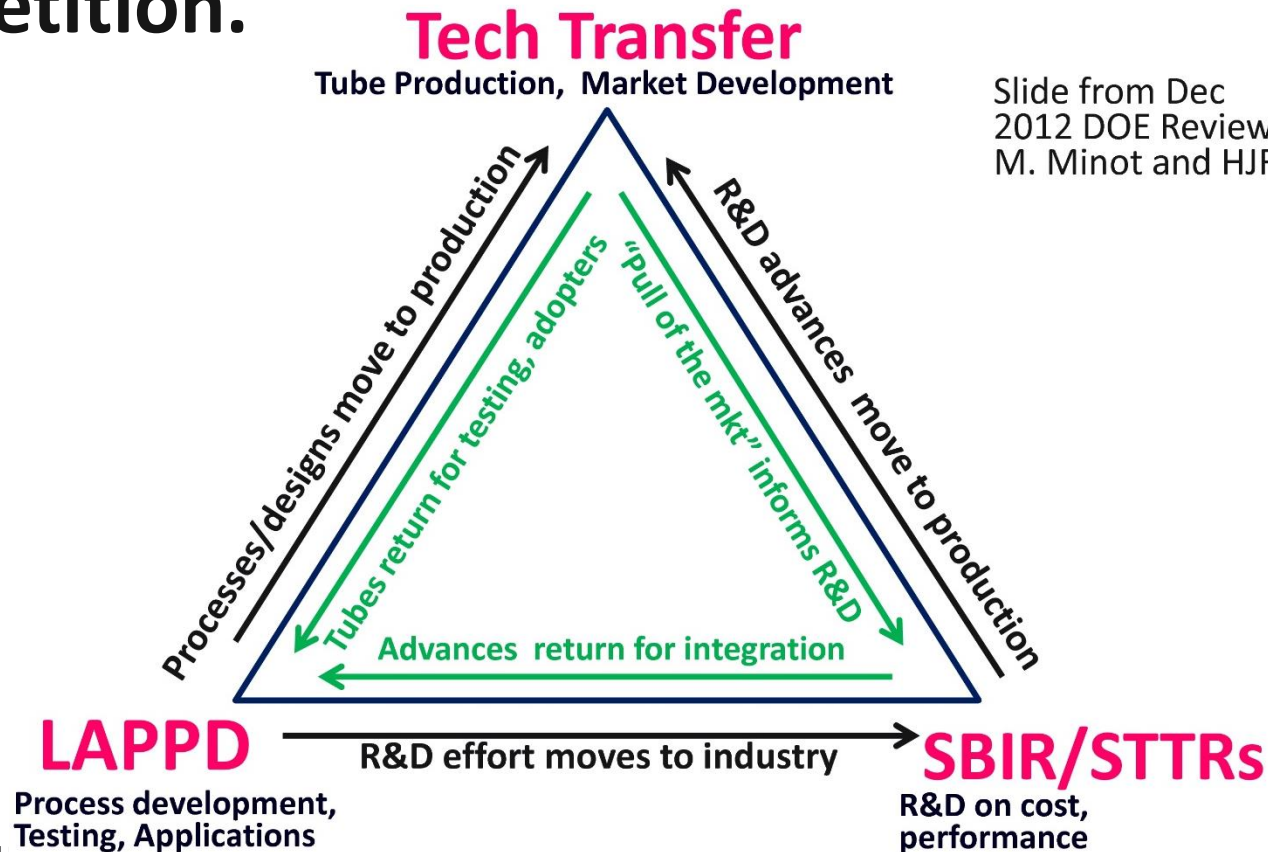
Part III. Advanced Designs and Fabrication



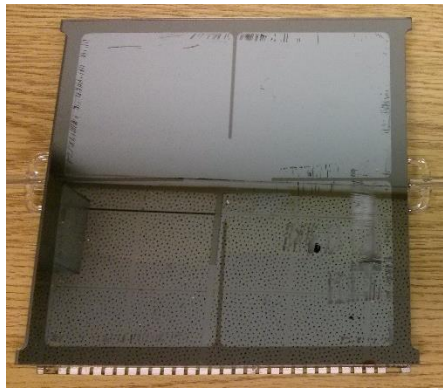
IMO all the performance parameters and single steps have been proven (and published) by the collaboration; the main problems we face are related to manufacturability.

Rationale for Gen-II

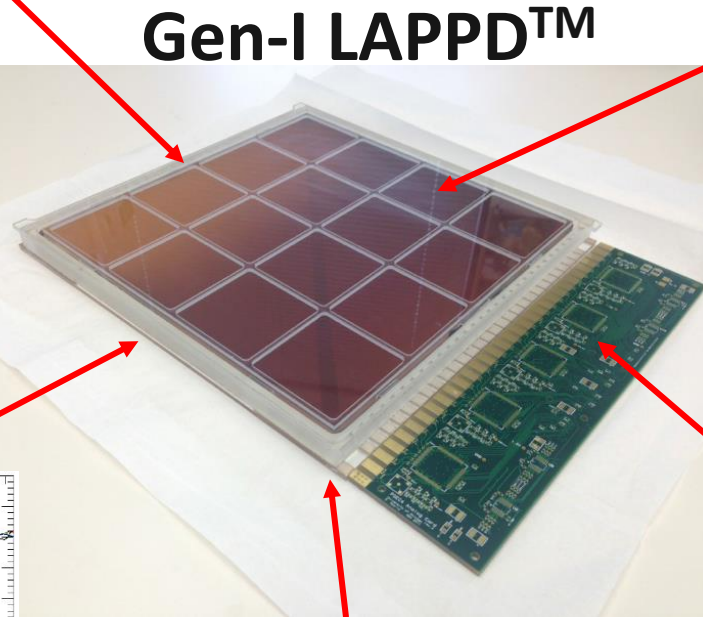
For LAPPDTMs to be useful to the HEP, Nuclear, and security communities they have to be affordable- IMO at or less than a Planacon. All the cost at present is in the fabrication- the packaging components are cheap. Need to look ahead to competition.



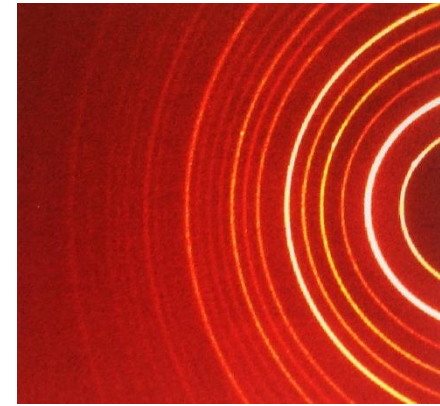
Toward an Affordable Gen-II Design



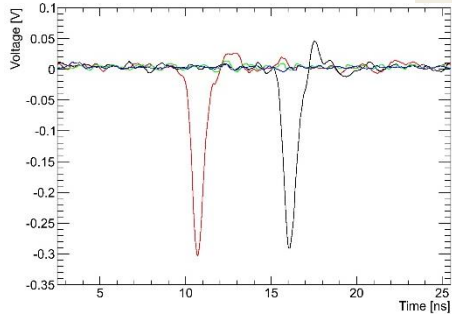
Flat Top Seal



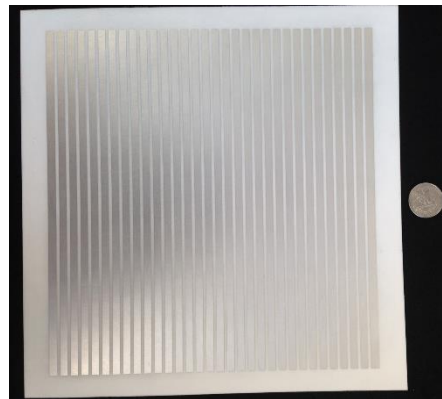
Gen-I LAPPD™



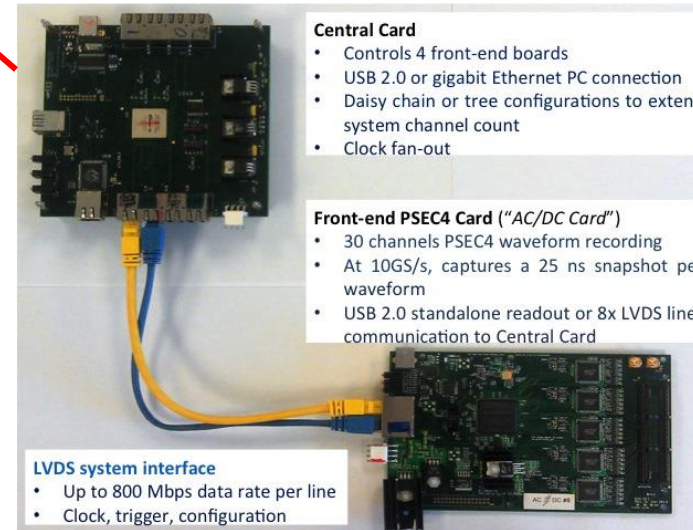
**High QE Photocathode
(patent with BNL, RMD)**



**Performance:
HV and signal
(NIM-A, RSI papers,
patent)**



High-BW ceramic pkg



Central Card

- Controls 4 front-end boards
- USB 2.0 or gigabit Ethernet PC connection
- Daisy chain or tree configurations to extend system channel count
- Clock fan-out

Front-end PSEC4 Card ("AC/DC Card")

- 30 channels PSEC4 waveform recording
- At 10GS/s, captures a 25 ns snapshot per waveform
- USB 2.0 standalone readout or 8x LVDS line communication to Central Card

LVDS system interface

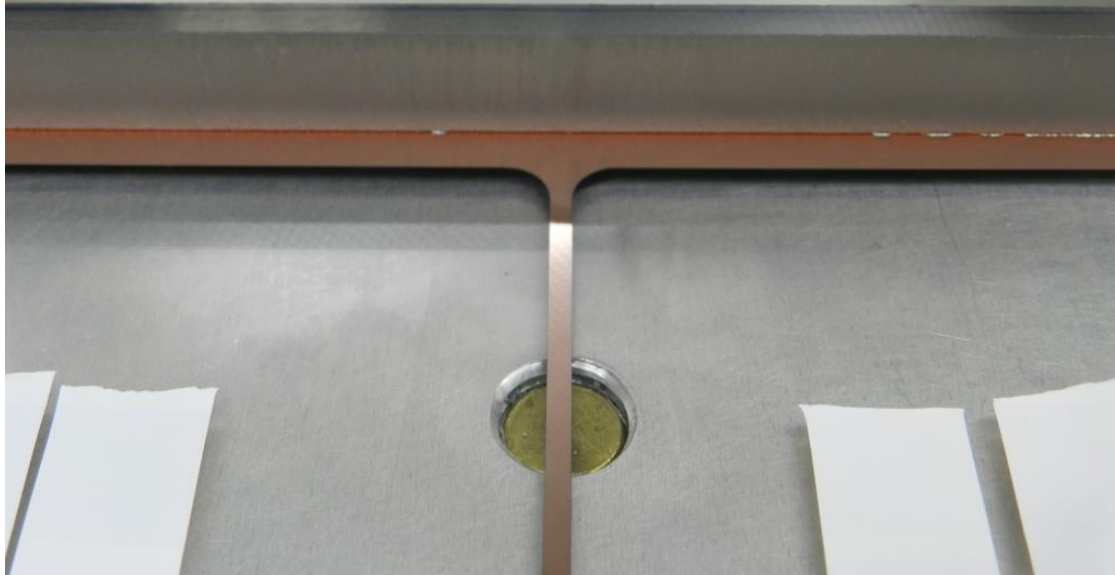
- Up to 800 Mbps data rate per line
- Clock, trigger, configuration

**Psec Electronics system
(NIM-A paper)**

Flat Indium Solder Seal

Andrey Elagin, Eric Spieglan,
Matt Wetstein

Sidewall seal seen
through window

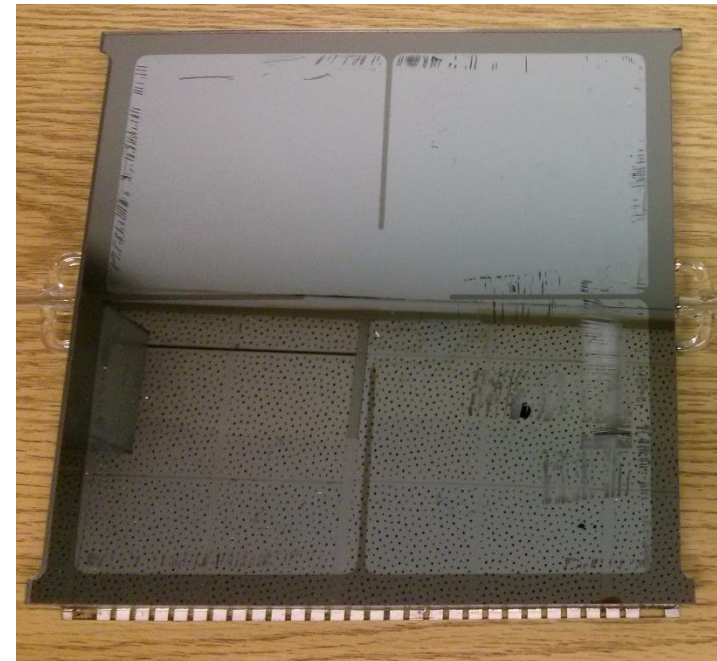


- No machining of glass groove
- No bulk flow if not level over 8"
- No manipulation of window

HOWEVER

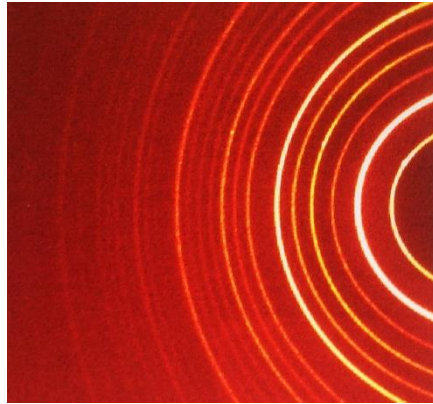
- Easiest with PMT-like cathode fabrication ('in situ')
- We do not completely understand the metallurgy yet

Sealed LAPPD™



Advanced Photocathode R&D

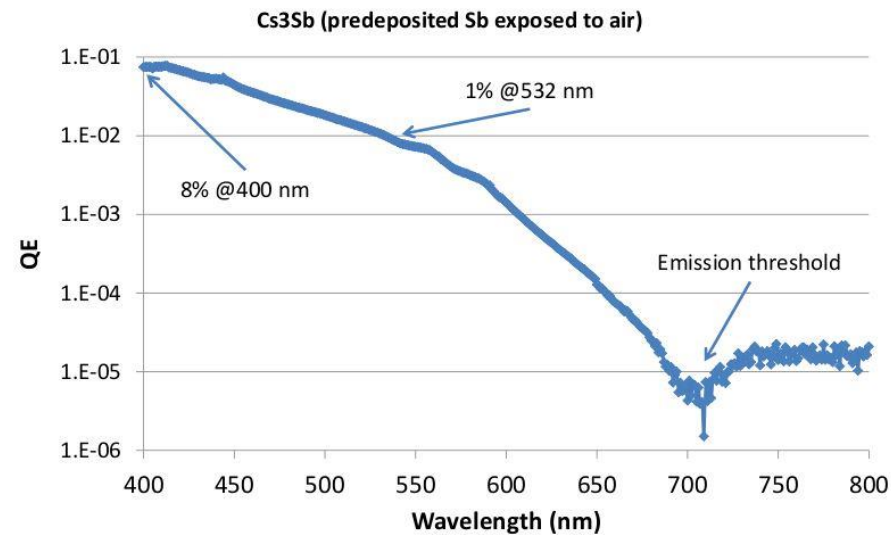
I. With RMD and BNL (SBIR) we have synthesized the stoichiometric compound K_2CsSb .



Powder diffraction Xray taken with new UC Bruker- 15nm nanocrystals of >99% pure K_2CsSb . Currently learning to sputter it. New kind of bulk material- semiconductor.

II. PMT-process production of photocathodes (with Luca Cultrera, Ivan Bazarov, Cornell)

- Exposure of predeposited Sb layer to Cs-K2 vapor makes a good K_2CsSb cathode (Singer, Sinclair)
- Cultrera has shown that air-exposed Sb produces a competitive Cs_3Sb photocathode.



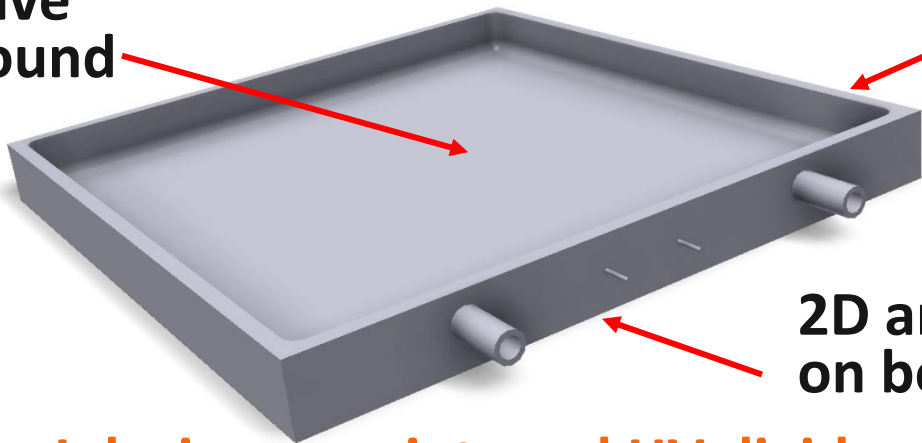
Credit: Luca Cultrera

Monolithic Capacitively-Coupled Ceramic

LAPPD™

Resistive or thin
Conductive
inner ground
layer

Green-trimmed full-
fire monolithic
ceramic LAPPD™ tile
base assembly



2D array of pads for readout
on bottom (**outside**) layer

- UC Gen-I design uses internal HV divider with HV applied through metalized window border and anode strips that extend through the bottom frit seal for DC gd and signal outputs - no external pins
- We are exploring a Gen-II ceramic design that allows pads for high-occupancy applications to solve the 'disambiguation' problem and that should have X3 the bandwidth, and requires no fritting. (Ceramic is also much stronger than glass) Could be used with Incom mini-SSL transfer process. In the middle of specifying for quotes- present status:

Quote	Unit Price (100)	NRE
Company A	\$314	\$2150
Company B	\$218	\$700

'Ultralight' R&D Fabrication Facility

Outer vacuum for seal process

Standard 16.5" ConFlat flange

Tile fixture heated (350C) by quartz lamps underneath

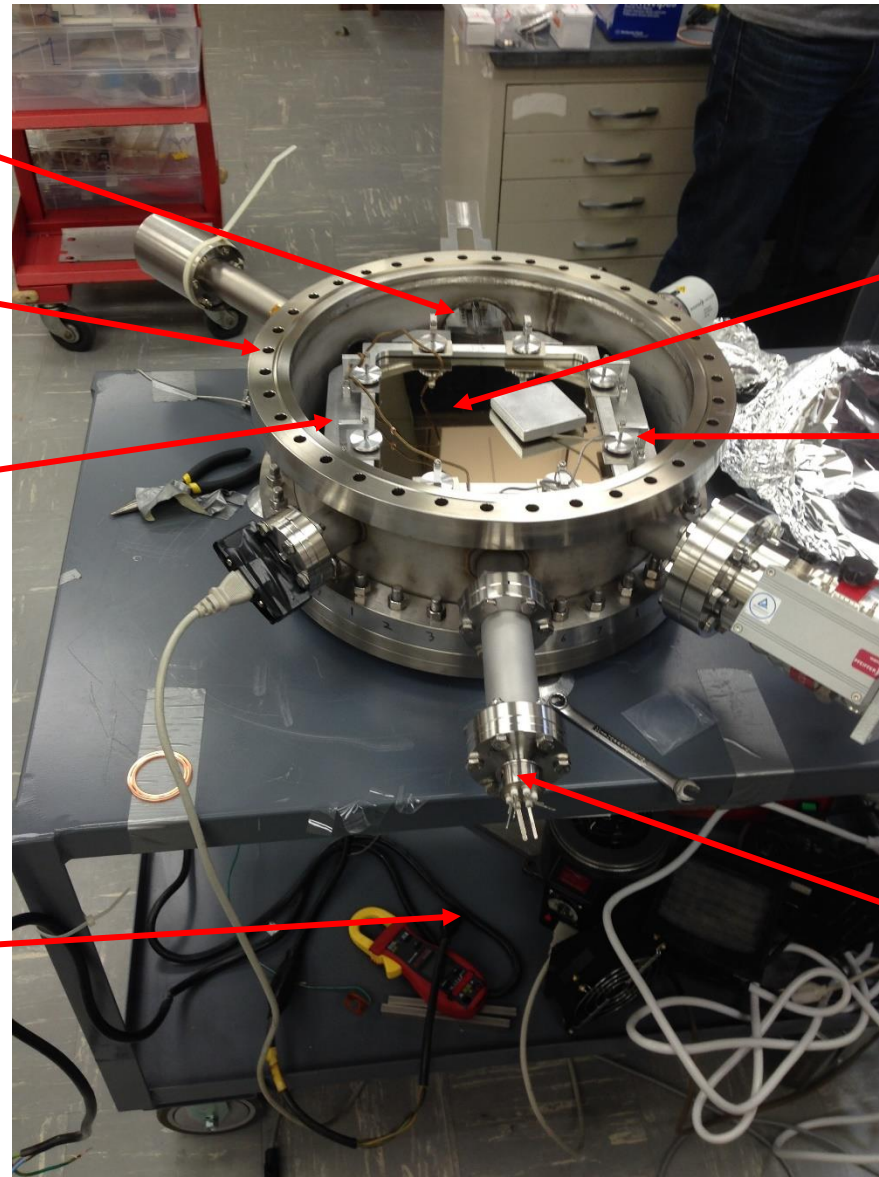
Raspberry Pi process data logger-temperatures (10), pressures, RGA,...

Sealed tile (no getter this shot)

Precision load and positioning fixture for seal

RGA on outer vacuum (for now)

Inner vacuum to tile and for bi-alkali vapor



NAIP: Arrows are messed up- don't believe them.

Radical and risky, but scaleable, fast thermal cycle, and based on commercial PMT production process (Burle)

UC Needs post-2015-ARL SOW & Budget

There have been two rapid technical developments since we submitted the 2015 SOW and Budget to ARL:

1. Eric has proposed PSEC-4A (deadtimeless) as an intermediate step to PSEC-5 , and available sooner;
2. With ceramics vendors we are developing a design the green-trim ceramic tile base assembly and it's surprisingly economical, higher performance, and seems viable.

We would like to ask in the near future for additional funds to do the exploratory work for each of these. We are in the middle of getting bids on the latter and Eric is deep in writing his thesis— at this point can only estimate the budgets:

Estimated Requests

- | | |
|---------------------------------------|-------|
| 1. PSEC-4A: 3 mo. Elec. Eng. | 48K\$ |
| 2. Ceramic LAPPD™ TBA's: 4 iterations | 24K\$ |

Brief Summary

- 1. The water-based Optical Time Projection Chamber concept works nicely and the results agree with Monte-Carlo-based expectations;**
- 2. PSEC-4 has been adopted by several groups and a number of others have Eval Cards; Iowa/MIT/Sandia-NM/Sandia-CA/UC have ordered 1200 more chips.**
- 3. We are progressing making the glass LAPPDT^{Ms} in the Ultralight scalable tile facility . We can consistently make flat hot seals for the LAPPDTM tiles; working with Indium Corp on intermetallic issues (confidential).**
- 4. Cornell has promising results on the photocathode process needed for the Ultralight facility ; separately with RMD and BNL we have synthesized the stoichiometric compounds and sputtered alkali cathodes;**
- 5. We are still in early stages of developing the Gen-II ceramic Tile Base Assembly, but it looks very attractive.**

Our Published PSEC Papers-p1

MCP Timing Performance : B.W. Adams, A. Elagin, H. Frisch, R. Obaid, E. Oberla, A. Vostrikov, R. Wagner, J. Wang, M. Wetstein; [Timing Characteristics of Large Area Picosecond Photodetectors](#) Nucl. Instr. Meth. Phys. Res. A. , Vol. 795, pp 1-11 (tbp Sept. 2015); pub.online **June 5, 2015**.

Fast Timing in Searches for Double Beta Decay C. Aberle, A. Elagin, H.J. Frisch, M. Wetstein, L. Winslow. [Measuring Directionality in Double-Beta Decay and Neutrino Interactions with Kiloton-Scale Scintillation Detectors](#); JINST 9 P06012 doi:10.1088/1748-0221/9/06/ (June 2014)
P06012arXiv:1307.5813

No-pin Internal HV Circuit B. W. Adams, A. Elagin, J. W. Elam, H. J. Frisch, J.-F. Genat, J. S. Gregar, A. U. Mane, M. J. Minot, R. Northrop, R. Obaid, E. Oberla, A. Vostrikov, M. Wetstein; [An Internal ALD-Based High Voltage Divider and Signal Circuit for MCP-based Photodetectors](#)}Nucl. Instr. Meth. Phys. Res. A; Vol. 780, Pages 107-113 (**April 2014**)

PSEC-4 Waveform Sampling Chip E. Oberla, J.-F. Genat, H. Grabas, H. Frisch, K. Nishimura, and G Varner
[A 15 GSa/s, 1.5 GHz Bandwidth Waveform Digitizing ASIC](#);
Nucl. Instr. Meth. A735, **Jan., 2014**,
<http://dx.doi.org/10.1016/j.nima.2013.09.042>;
<http://arxiv.org/abs/1309.4397>

Our Published PSEC Papers –p2

MCP Testing and Pulse Performance : B. Adams, M. Chollet, A. Elagin, A. Vostrikov, M. Wetstein, R. Obaid, and P. Webster
A Test-facility for Large-Area Microchannel Plate Detector Assemblies using a Pulse Sub-picosecond Laser;
Review of Scientific Instruments **84**, 061301 (**Oct. 2013**)

Microstrip Anode RF Performance H. Grabas, R. Obaid, E. Oberla, H. Frisch J.-F. Genat, R. Northrop, F. Tang, D. McGinnis, B. Adams, and M. Wetstein;
RF Strip-line Anodes for Psec Large-area MCP-based Photodetectors,
Nucl. Instr. Meth. A71, pp124-131, **May 2013**

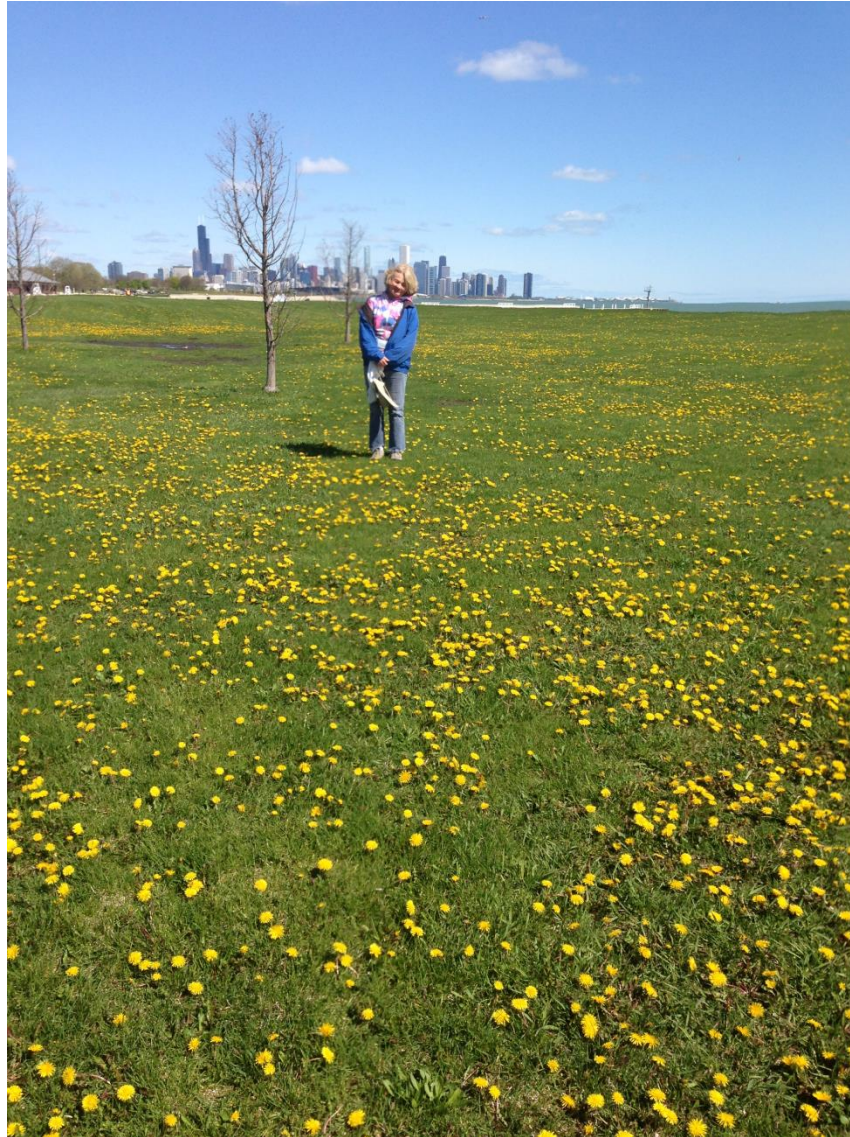
In Preparation

The OTPC E. Oberla et al.
Performance of a Prototype Optical Time Projection Chamber; to be submitted to
Nucl. Instr. Meth. **summer 2015**

Many Thanks to:

- **Our Collaborators** at ANL-ESD, ANL-XSD, ANL-MSD, UC-Berkeley SSL, Hawai'i, BNL and Cornell (esp. Joe Gregar, Ossy, Gary, Klaus, Bernhard, and Luca)
- **Staff and management at Incom, Arradiance, InnoSys, and RMD corporations (esp. Michael)**
- **The Fermilab Mcenter Test Beam Crew and LArIAT (esp. JJ)**
- **Others in the field of fast-timing , with special thanks to T. Ohshima and J. Vavra; and waveform sampling, (special thanks here to D. Breton, E. Delagnes, J.F.-Genat, S. Ritt, and G. Varner)**
- **Howard Nicholson and the US DOE Office of HEP; Shawn, John, and the ARL staff**
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The End



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